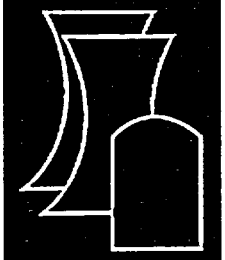
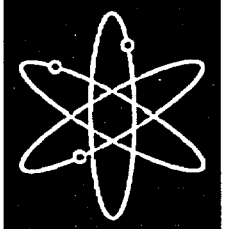
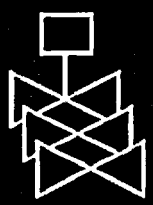
NUREG-1709







Selection of Sample Rate and Computer Wordlength in Digital Instrumentation and Control Systems

U.S. Nuclear Regulatory Commission
Office of Nuclear Regulatory Research
Washington, DC 20555-0001

AVAILABILITY OF REFERENCE MATERIALS IN NRC PUBLICATIONS

NRC Reference Material

As of November 1999, you may electronically access NUREG-series publications and other NRC records at NRC's Public Electronic Reading Room at www.nrc.gov/NRC/ADAMS/index.html. Publicly released records include, to name a few, NUREG-series publications; *Federal Register* notices; applicant, licensee, and vendor documents and correspondence; NRC correspondence and internal memoranda; bulletins and information notices; inspection and investigative reports; licensee event reports; and Commission papers and their attachments.

NRC publications in the NUREG series, NRC regulations, and *Title 10, Energy*, in the Code of *Federal Regulations* may also be purchased from one of these two sources.

1. The Superintendent of Documents
   U.S. Government Printing Office
   P. O. Box 37082
   Washington, DC 20402–9328
   www.access.gpo.gov/su_docs
   202–512–1800
2. The National Technical Information Service
   Springfield, VA 22161–0002
   www.ntis.gov
   1–800–553–6847 or, locally, 703–605–6000

A single copy of each NRC draft report for comment is available free, to the extent of supply, upon written request as follows:

Address: Office of the Chief Information Officer,
Reproduction and Distribution
Services Section
U.S. Nuclear Regulatory Commission
Washington, DC 20555-0001
E-mail: DISTRIBUTION@nrc.gov
Facsimile: 301–415–2289

Some publications in the NUREG series that are posted at NRC's Web site address www.nrc.gov/NRC/NUREGS/indexnum.html are updated regularly and may differ from the last printed version.

Non-NRC Reference Material

Documents available from public and special technical libraries include all open literature items, such as books, journal articles, and transactions, *Federal Register* notices, Federal and State legislation, and congressional reports. Such documents as theses, dissertations, foreign reports and translations, and non-NRC conference proceedings may be purchased from their sponsoring organization.

Copies of industry codes and standards used in a substantive manner in the NRC regulatory process are maintained at—

The NRC Technical Library
Two White Flint North
11545 Rockville Pike
Rockville, MD 20852–2738

These standards are available in the library for reference use by the public. Codes and standards are usually copyrighted and may be purchased from the originating organization or, if they are American National Standards, from—

American National Standards Institute
11 West 42nd Street
New York, NY 10036–8002
www.ansi.org
212–642–4900

The NUREG series comprises (1) technical and administrative reports and books prepared by the staff (NUREG–XXXX) or agency contractors (NUREG/CR–XXXX), (2) proceedings of conferences (NUREG/CP–XXXX), (3) reports resulting from international agreements (NUREG/IA–XXXX), (4) brochures (NUREG/BR–XXXX), and (5) compilations of legal decisions and orders of the Commission and Atomic and Safety Licensing Boards and of Directors' decisions under Section 2.206 of NRC's regulations (NUREG–0750).

NUREG-1709

Selection of Sample Rate and Computer Wordlength in Digital Instrumentation and Control Systems

Manuscript Completed: June 2000
Date Published: July 2000

Prepared by
T. W. Jackson

Division of Engineering Technology
Office of Nuclear Regulatory Research
U.S. Nuclear Regulatory Commission
Washington, DC 20555-0001

ABSTRACT

Digital sampling of analog signals adds two types of errors, aliasing and finite wordlength error, to the sampled version of the signal. Aliasing is characterized by high frequency components misrepresented as low frequency components in the sampled signal. It is greatly influenced by the sample rate, and may lead to degraded performance in monitoring, alarm, control, and protection systems. Since computer wordlengths are finite in length, digital systems are limited in their capability to represent real number values. Finite wordlength errors related to round-off, truncation, and data conversion have the potential to adversely impact the performance of digital instrumentation and control (I&C) systems. The Office of Nuclear Regulatory Research is investigating good engineering practices regarding aliasing and finite wordlength errors in nuclear facilities. Hazards associated with these errors are minimized through proper design and selection of sample rates and computer wordlengths. This document provides the regulatory background, theoretical information, practical issues, best engineering practices, and examples associated with sample rate and computer wordlength selection.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

EXECUTIVE SUMMARY

Background

Digital instrumentation and control (I&C) equipment continues to replace aging analog I&C equipment in commercial nuclear facilities. From a functional point of view, digital and analog I&C equipment are similar, with the exception of some functional enhancements found in digital I&C. However, operational aspects of the two technologies are very different. For example, software logic operates in sequential fashion, whereas analog circuitry operates in parallel. This document focuses on one operational difference: the conversion of analog signals to binary numbers by digital I&C systems, and the use of these numbers to calculate results.

Digital I&C systems manipulate binary numbers, but they interact with physical, real-world systems. They convert analog signals to binary numbers, and in many cases convert binary results back to analog signals. A special device, called an *analog-to-digital (A/D) converter*, samples the analog signal and produces a binary number corresponding to its value. Two key factors are important to the performance, reliability, and safety of digital I&C systems. One factor is the rate at which analog signals are digitized (*sample rate*), and the other factor is the maximum number of binary place values (*wordlength*) representing real-number values. Sample rate and computer wordlengths are not a factor of consideration in analog I&C systems.

Problem

Problems arise when analog signals are not sampled fast enough. When a digital I&C system samples, it gets a snapshot of the analog signal at discrete time intervals. If the signal changes rapidly and the sample time intervals are not small enough, the sampled version of the signal will misrepresent high frequency components of the original signal as low frequency components. This type of signal corruption is called *aliasing*.

Other problems arise from the binary representation of real-world numbers. Computers represent real numbers with a finite number of binary place values, or *wordlength*. Because of finite wordlengths, mathematical operations such as addition and multiplication introduce round-off and/or truncation errors. If *finite wordlength errors* are not properly addressed in digital I&C systems, they can cause unexpected behavior.

Safety Significance

The problems mentioned above are potential hazards for nuclear I&C systems. In control systems, aliasing or severe finite wordlength errors may cause instability. In monitoring, alarm, and protection systems, such conditions degrade performance. For protection systems in particular, aliasing and finite wordlength errors may cause the system to violate its setpoint accuracy requirements. However, these error sources can be minimized to a point in which they have an insignificant effect on system performance. The following is a summary of methods and practices to minimize aliasing and finite wordlength effects.

Sample Rate Selection

Sample rate selection for a particular signal depends upon its rate of change (frequency content of the signal). *Shannon's Sampling Theorem* states that a signal must be sampled two times faster than the signal's highest frequency component to reconstruct the signal in the time domain. This theorem defines a theoretical minimum sample rate to prevent aliasing. When practical issues, such as signal noise, are considered, the sample frequency is greater than two times the highest frequency of the analog signal. Calculation of the minimum sample rate depends upon the following:

1. Application — control, monitoring, protection, or indication

2. Environment — signal noise

3. I&C equipment — input signal filters, A/D converters, and other interfacing computer equipment

4. Interfacing systems — actuators and dynamics of the plant process

This document presents sample rate selection methods for various types of digital I&C systems found in nuclear facilities. These systems include *discrete*, *open-loop*, and *closed-loop I&C systems*. Discrete I&C systems deal with input signals taking on one of two values, and the input signals often come from discrete devices such as relays, bistables, etc. Discrete I&C systems do not have aliasing problems, but the selected sample rate may be influenced by response-time requirements.

Open-loop I&C systems do not have feedback signals and include protection, monitoring, alarm, and some control systems. Three sample rate selection methods are commonly used with open-loop I&C applications. Two of the methods, the *sampling ratio method* and the *oversampling method*, are concerned with meeting a maximum allowable aliasing level, and they are best suited for those systems requiring signal accuracy. In the document, calculations and procedures describe the appropriate ways of using these methods. A third method, the *rise-time method*, is suitable for open-loop I&C systems that do not have stringent signal accuracy requirements.

Closed-loop I&C systems have at least one feedback signal and deal mostly with closed-loop control. There are three sample rate selection methods available to closed-loop I&C systems: the *phase/gain margin method*, the *closed-loop bandwidth method*, and the *rise-time method*. These methods are mainly concerned with system stability, although aliasing may be a problem in these systems also.

The following design considerations (DC) are commonly considered by digital designers when selecting sample rates:

- DC1: The A/D converter's least significant bit (LSB), linearity, offset, and gain error are potential sources of signal error.
- DC2: Sample rate selection is influenced by response-time requirements of the digital system.
- DC3: Accuracy of input signals is affected by the level of aliasing.
- DC4: Typically, the worst-case transient frequency spectrum (including the signal bandwidth and high frequencies), the type of anti-aliasing filter, and the allowable aliasing level are inputs to the sample rate selection process for open-loop systems.
- DC5: When the sampling ratio method is used for sample rate selection, the following assumptions are evaluated for their validity: (1) frequencies beyond the signal bandwidth are lower in magnitude than those within the bandwidth and (2) the cutoff frequency of the anti-aliasing filter is equal to the signal bandwidth.
- DC6: Sample rate selection calculations describe how the chosen sample rate and anti-aliasing filter meet the allowable aliasing requirements.
- DC7: When the oversampling method is used, the sample rate is sufficiently high enough that resulting aliasing is below allowable requirements.
- DC8: When the oversampling method is used, it may capture a large amount of high frequencies that could affect downstream plant equipment.
- DC9: The adequacy of sample rates in closed-loop control systems may be determined by the phase/gain margin.
- DC10: If the closed-loop bandwidth method is used for sample rate selection in closed-loop systems, the sample rate is typically six times higher than the closed-loop bandwidth.
- DC11: If the rise-time method is used for sample rate selection in closed-loop systems, the number of samples per rise time is typically greater than or equal to four.

Computer Wordlength Selection

Finite wordlength errors occur when real-number data are represented by a finite number of bits in a computer system. These errors occur at input signal acquisition, intermediate calculations, the output signal, and algorithm coefficients. For example, finite wordlength errors are introduced at A/D conversion. The accuracy of the conversion is impacted by the A/D converter's *dynamic range*. As the converter covers a wider range of input values and resolves to smaller voltage levels, the dynamic range increases. The dynamic range is affected by the wordlength of the A/D converter and its associated error specification.

Intermediate calculations are affected by finite wordlengths of computer memory. Errors associated with intermediate calculations include round-off/ truncation error, *overflow*, and incorrect type conversion. Overflow occurs during addition when the result occupies one more bit than the available storage space. Incorrect type conversions may occur when numbers are converted between two different numbering conventions (i.e., fixed- and floating-point notation).

In many applications, digital I&C systems convert digital results into analog signals. The conversion is carried out using a *digital-to-analog (D/A) converter.* Because the value of the digital signal is not known between updates, the D/A converter accepts a digital value and holds it at a representative DC voltage until the next update arrives. This creates a step-like analog signal that may not be acceptable to some plant systems. By increasing the update time and/or wordlength, or placing an analog filter at the D/A converter's output, a smoother analog signal is produced.

Often, when algorithms are developed for digital I&C systems, real-number coefficients are used in the design. When the coefficients are placed into the digital I&C system. truncation or round-off of the coefficients may occur, potentially degrading system performance. This type of error is more likely to occur if the system uses complex algorithms.

The following design considerations (DC) are commonly considered by digital designers when selecting computer wordlengths:

- DC12: Dynamic range and headroom are two computer wordlength considerations when A/D converters are specified.
- DC13: Overflow, round-off/truncation, resolution, and type/size conversion of fixed- and floating-point numbers are potential sources of computer wordlength errors.
- DC14: Compatibility of analog output signals with downstream electrical/electronics systems are a consideration with D/A converter selection and installation. Areas of compatibility include signal shape, rate of change, range, and power level.
- DC15: Finite wordlength effects on algorithm coefficients may affect the accuracy of computer calculations.

This document reviews back-ground regulatory information and provides the technical bases for sample rate and computer wordlength selection. Such information would be used by NRC staff during their review of digital I&C systems in nuclear power plants.

ACKNOWLEDGMENTS

This research was conducted as a joint in-house effort between the Office of Nuclear Regulatory Research and the Office of Nuclear Reactor Regulation. The support and technical review by Mr. John A. Calvert, Mr. James C. Stewart, Mr. Clifford K. Doutt, and others are greatly appreciated. Thanks are also due to Mr. Fuat (Frank) Odar at the NRC and the staff at the NRC Technical Training Division for supplying simulation results for use in the case studies.

1 INTRODUCTION

1.1 Background

Digital instrumentation and control (I&C) system upgrades continue in nuclear facilities as older, analog I&C systems become more difficult to maintain. Although both types of I&C systems perform similar functions, there are many differences in their operating characteristics (National Research Council, 1997). For example, digital I&C systems contain software and perform complex functions in a sequential, versus parallel operation found in analog I&C systems. Regulatory documents addressing this and other differences ensure that new hazards associated with digital I&C systems do not enter nuclear facilities (USNRC, 1997a).

One key difference between digital and analog I&C systems is the way they acquire plant input signals. Figure 1.1 illustrates this difference. Analog I&C systems directly use the voltage/current value of plant input signals to compute results. On the other hand, digital I&C systems convert voltage/current values of plant signals into a string of binary numbers. This string of binary numbers is called a *digital signal.* The device that converts analog signals to digital signals is called an *analog-to-digital* (A/D) *converter.* After signal conversion, results are calculated using the digital signal, and the digital result may or may not be converted back to an analog signal. The device that converts digital signals to analog signals is called a *digital-to-analog* (D/A) *converter.*

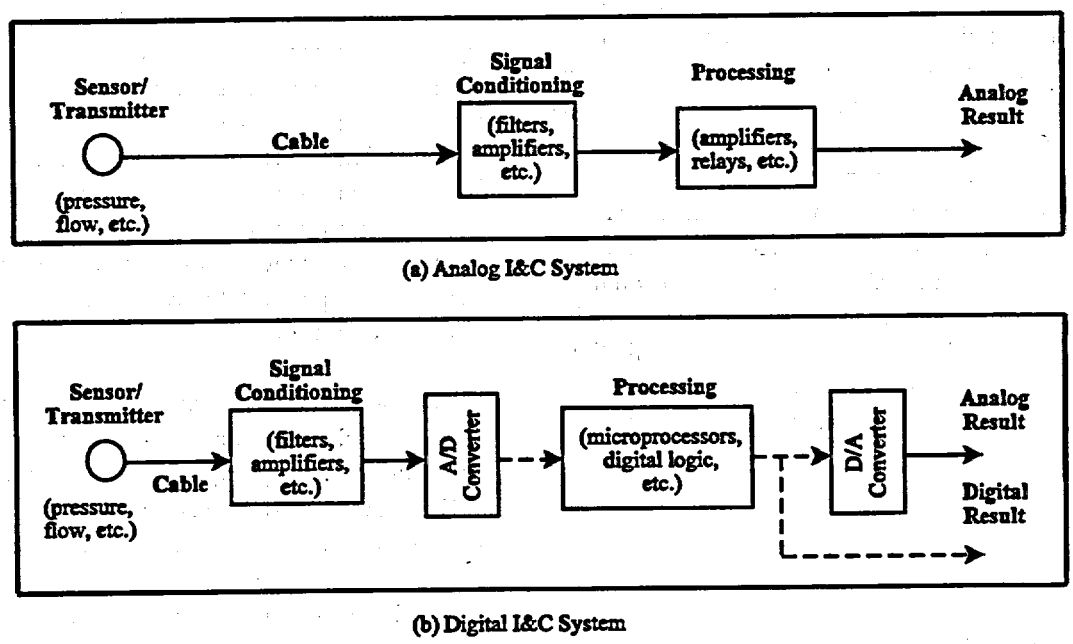


Figure 1.1 Comparison of analog and digital I&C systems

With digital safety systems, two hazards, *aliasing* and *finite wordlength errors*, need to be addressed. Aliasing occurs at A/D conversion. When the A/D converter samples the analog signal at fixed time intervals, each sample is represented by a binary number. Between sampling intervals, the value of the analog signal is unknown to the digital I&C system. If the analog signal changes significantly between samples, the digital signal will not adequately represent it. In this case, high frequency components of the analog signal are falsely represented as lower frequency components in the digital signal. This false representation of frequencies is called aliasing, and it has the potential to degrade input signals to digital safety systems.

The second hazard involves finite wordlength effects in digital I&C systems. In computers, binary numbers have a finite number of place values, or *bits*. The number of bits representing a value is called the *wordlength*. Common computer wordlengths include 8, 16, and 32 bits. Resolution errors are created when analog signals, which represent real-number values, are converted to binary numbers having finite wordlength. Finite wordlengths also create truncation and round-off errors in basic mathematical operations. If properly addressed, finite wordlength errors do not significantly affect digital I&C systems. However, severe finite wordlength errors may lead to oscillations and discontinuous jumps in control systems and degraded performance in monitoring, alarm, and protection systems.

1.2 Purpose

The motivation of this report is to address the inconsistency concerning sample rate and computer wordlength selection. In past reviews, the NRC Staff has encountered various techniques and methodologies for sample rate selection; some having little technical bases. In state-of-the-practice digital design, there are processes for sample rate selection based on engineering principles. For the NRC staff to gain adequate confidence in the safety of digital systems, it is important to use technically sound engineering processes to demonstrate the quality and reliability of such systems. The purpose of this document is to outline those engineering processes.

1.3 Scope

This document is intended to provide technical basis for NRC staff when reviewing digital I&C equipment in nuclear facilities. The review of digital I&C equipment involves many issues, two of which include sample rate and computer wordlength selection. The review of sample rate and computer wordlength selections is conducted at the same time other real-time computer issues are investigated. While the review of sample rate and computer wordlength selection is somewhat independent of other digital I&C system issues, the topics discussed in this document may influence other digital review issues such as requirements specifications and data communications. The goal of this document is to provide technical information on proper sample rate and computer wordlength selection. While aliasing and finite wordlength errors can never be eliminated, they can be minimized through proper design and equipment selection.

It is important that each application be reviewed in its own light since aliasing and finite wordlength errors are affected by requirements, characteristics, I&C equipment, and the environment of the particular system. In other words, some of the sample rate and computer wordlength issues can be addressed on a generic level by vendors, however, the final application will influence the decision for sample rate and computer wordlength selections.

This document does not address the following: (1) other real-time computer issues (unless they impact, or are impacted by, sample rate and computer wordlength selection); or (2) analog issues related to sensors, transmitters, cables, or signal conditioners.

This document does not address sample rate and computer wordlength selection from a risk perspective for two reasons. First, aliasing and finite wordlength errors are design issues, and, if the design is not performed correctly, risk is difficult to assess. Second, risk is different for each digital I&C system since it depends upon the plant system in which it resides.

It is assumed the reader has a basic knowledge of electrical engineering principles, including signal filters, frequency spectrum/response, signal converters, and digital logic. Some of this basic knowledge is supplemented in the text and appendices, while more basic and advanced information is provided in the references.

1.4 Report Organization

This report provides the technical bases for the review of sample rate and computer wordlength selection. The technical bases are indicated as design considerations, which are marked by the letters "DC#," with "#" identifying the number.

In Chapter 2, the relation between aliasing and finite wordlength errors and response-time and setpoint accuracy requirements is presented. Included in this chapter are references to applicable regulations, regulatory guides, and standards.

Chapter 3 presents the necessary technical information and review guidelines; including Shannon's Sampling Theorem, anti-aliasing filters, and equations to determine the minimum required sample rate for an application.

Chapter 4 provides the technical basis related to finite wordlength effects. Such topics include finite wordlength effects on input, intermediate, and output signals, as well as algorithm coefficients.

Chapter 5 summarizes the technical bases presented in the previous chapters.

Six appendices provide additional information regarding sample rate and computer wordlength selection. Appendix A contains an overview of different A/D converters. Appendix B states the mathematical basis for digital sampling and Shannon's Sampling Theorem. Appendix C offers an overview of various anti-aliasing filters. Appendix D presents different aspects of frequency spectrums, including the Fourier Transform and methods to obtain the frequency spectrum. Appendix E illustrates sample rate selection and aliasing in a digital pressurized water reactor (PWR) protection system. And finally, Appendix F illustrates sample rate selection effects in a digital steam generator level control system.

2 REGULATORY BACKGROUND

Aliasing and *finite wordlength* errors are known to cause failures in digital I&C systems (USNRC, 1997b, 1998). Because of the inability to totally eliminate them, it is important to discuss the regulatory basis for reviewing such error sources. Two requirements, setpoint accuracy and response-time of nuclear protection systems, are affected by aliasing and finite wordlength errors. This chapter makes reference to regulations, regulatory guides, and standards addressing setpoint accuracy and response-time requirements. Emphasis is placed on the relationship between these requirements and aliasing and finite wordlength errors.

2.1 Setpoint Accuracy

This section addresses the impact of aliasing and finite wordlength errors on setpoint accuracy. Instrument setpoints determine when nuclear *safety-related systems* engage as a result of adverse plant conditions. Because of setpoint drift and other numerical/signal errors, a safety-related system may not engage within its specified engagement band. Realizing the potential consequences, the following regulations address the issue of setpoint accuracy:

- 10 CFR 50.55a(h), "Protection systems,"
- 10 CFR 50.36(c)(1)(ii)(A), "Technical specifications,"
- 10 CFR Part 50, Appendix A, General Design Criteria (GDC) 10, "Reactor Design,"
- 10 CFR Part 50, Appendix A, GDC 12, "Suppression of Reactor Power Oscillations,"
- 10 CFR Part 50, Appendix A, GDC 13, "Instrumentation and Control," and
- 10 CFR Part 50, Appendix A, GDC 20, "Protection System Reliability and Testability."

Regulatory Guide 1.105, "Instrument Setpoints for Safety-Related Systems," describes a method acceptable to the NRC staff for complying with the regulations to ensure that instrument setpoints are initially within, and remain within, technical specification limits (USNRC, 1986). This regulatory guide endorses ISA-S67.04-1982, "Setpoints for Nuclear Safety-Related Instrumentation Used in Nuclear Power Plants (ISA, 1982)."[1] This standard specifies methods for combining uncertainties (errors) to determine trip setpoints and their allowable value. If instrument setpoints drift outside their allowable value, those protection channels are inoperable. To keep all protection channels operable, the NRC sets a probability limit of 95% on the distribution of errors that cause a setpoint to drift beyond its allowable limit. In other words, 95% of the error data points are bounded below the allowable limit by the trip setpoint value selected.

Aliasing and finite wordlength errors contribute to uncertainty in setpoint calculations. For example, aliasing causes digital I&C systems to attribute lower, or higher deviations, to plant variables. Round-off and truncation also cause deviations in such variables. ISA-RP67.04-Part II-1994, Appendix H of that document lists aliasing, round off, and truncation errors as sources of uncertainty for setpoint calculations (ISA, 1994). Chapter 3 contains more detail on aliasing and its impact on setpoint accuracy. It also provides methods for aliasing measurement. Chapter 4 provides similar insight for finite wordlength errors.

---

[1] ANSI/ISA Standard S67.04-1994 is the revision to ISA S67.04-1982 (ANSI/ISA, 1994). At the time of publication, the NRC staff is proposing to update Reg. Guide 1.105 with the revised standard. However, differences between the Reg. Guide and standard revisions do not impact sample rate and computer wordlength discussion in this document.

2.2 Response-time Requirements

Response-time requirements ensure that automatic protection systems engage within an allotted time period to protect the fuel cladding, reactor pressure boundary, and/or containment. The following regulations apply to safety-related system response-time requirements:

- 10 CFR 50.55a(h), "Protection systems,"
- 10 CFR 50.36(c)(1)(ii)(A), "Technical specifications,"
- 10 CFR Part 50, Appendix A, GDC 12, "Suppression of Reactor Power Oscillations," and
- 10 CFR Part 50, Appendix A, GDC 20, "Protection System Reliability and Testability."

Several other regulatory documents and standards also provide guidance on response-time requirements. For example, 10 CFR 50.55a(h) endorses IEEE Std. 603-1991, "IEEE Standard Criteria for Safety Systems for Nuclear Power Generating Stations." This standard states in Section 4.10 that critical points in time should be specified for (a) initiation of protective action, (b) completion of protective action, (c) time when automatic control of protective action is required, and (d) time when protective action may be returned to normal (IEEE, 1991). ISA-S67.06-1984, "Response-Time Testing of Nuclear Safety-Related Instrument Channels in Nuclear Power Plants," describes a procedure for ensuring response-time requirements are accomplished (ISA, 1984).

Response-time requirements and aliasing prevention are two separate concerns. However, both concerns affect sample rate selection. With aliasing prevention, the sample rate is chosen to meet aliasing error requirements (see Section 2.1). When meeting response-time requirements, sample rates are chosen to meet the overall protection channel response time. For digital protection systems, the combination of sample rate, analog processing, and digital processing should be fast enough to meet both concerns. This is different from analog protection systems in which sample rate and digital processing were not a concern.

2.3 Other Documents

Both the selected sample rate and computer wordlength result in timing and architecture requirements. Review areas where such requirements may appear include the following.

Software Requirements Specifications

Computer wordlength selection may limit the types of operations and structure of algorithms for use on software variables [see BTP HICB-14, "Guidance on Software Reviews for Digital Computer-Based Instrumentation and Control Systems"] (USNRC, 1997a),

Real-Time Computer Requirements

Sample rate selection would impose timing requirements on computer operations [see NUREG/CR-6083, "Reviewing Real-Time Performance of Nuclear Reactor Safety Systems," and BTP HICB-21, "Guidance on Digital Computer Real-Time Performance,"] (USNRC, 1993a; USNRC, 1997a), and

Data Communication Requirements

Sample rate selection may impose timing requirements for the data communication system. Computer wordlength selection may impose requirements on data transmission equipment or protocols [see NUREG/CR-6082, "Data Communications"] (USNRC, 1993b).

While the SRP's main focus is on I&C safety-related systems, it also addresses non-safety-related I&C systems. The SRP mentions that many concepts in ANSI/IEEE Std. 279 are applicable to I&C systems for which high functional reliability is a goal

(ANSI/IEEE, 1971). Such systems are reviewed for the following reasons:

- Controlled variables remain in prescribed operating ranges.
- Operation and failure of these systems are bounded by accident analysis.
- Quality and reliability of these systems are sufficient to minimize challenges to safety-related systems.

For instance, improper sample rate selection in control systems causes instability. Although the control system is not a safety-related system, the instabilities may cause the plant to unnecessarily trip; thus challenging safety-related systems. Appendix F illustrates the effects of sample rate selection on a typical control system.

2.4 Safety Significance

The previous sections address sample rate and computer wordlength selection in light of regulations and acceptance criteria found in 10 CFR Part 50 and its supporting regulatory framework. As the NRC moves toward a risk-informed regulatory environment, sample rate and computer wordlength selection continue to be valid design issues. The following material describes the relation between risk-informed regulation and sample rate and computer wordlength selection.

At the present, it is difficult to assess the frequency and consequences of aliasing and finite wordlength error since few digital safety-related systems have been placed in nuclear power plants. However, in risk analysis, it is assumed that systems have been designed appropriately and fail in a random fashion. Since aliasing and finite wordlength errors are design errors, and not operational failures, they do not fail in a random fashion.

In the SECY paper, "Recommendations for Reactor Oversight Process Improvements," several cornerstones of safety are listed (USNRC, 1999). Two cornerstones, "limit the frequency of initiating events" and "ensure the integrity of the fuel cladding, reactor coolant system, and containment boundaries," have been compromised by inappropriate sample rate or computer wordlength selection, as shown in two past events. In one event, incorrect sample rate selection resulted in operation above rated power, which could challenge fuel cladding integrity (USNRC, 1998). In another event, incorrect sample rate selection for a digital integrated control system would cause unnecessary reactor trips (USNRC, 1997b). These events illustrate the impact of sample rate and computer wordlength selection on the cornerstones of safety.

2.5 Summary

Aliasing and finite wordlength errors affect setpoint calculations, response-time requirements, and other real-time parameters. Current regulations and guidance in the form of regulatory guides, standards, and the Standard Review Plan provide a basis for reviewing sample rate and computer wordlength selection in digital I&C systems. Aliasing and finite wordlength error cannot be totally eliminated. However, these effects should be addressed so that they do not affect plant safety. Because of the impact of some systems within nuclear power plants, the designer may need to evaluate the effects of aliasing and finite wordlength error in certain alarm, control, and monitoring systems.

3 SAMPLE RATE SELECTION

Sample rate selection is an important design decision for many digital instrumentation and control (I&C) systems. Unlike analog I&C systems, which use current and voltage signals directly, digital I&C systems represent analog plant signals using binary numbers. Crucial to digital I&C system design is the rate at which analog-to-digital (A/D) conversion occurs. This rate, known as the *sample rate*, affects the quality of the digitized plant signal. The sample rate is determined by the plant signal's rate of change and the I&C application requirements. If a plant input signal is not sampled fast enough, a phenomenon known as *aliasing* occurs. Aliasing produces error between the plant signal and its digital representation.

This chapter presents the technical basis for sample rate selection. The following three topics are discussed in order:

1. A/D conversion
2. Digital sampling and aliasing
3. Sample rate selection techniques

3.1 A/D Conversion

During A/D conversion, analog signals are represented by a set of binary numbers called a digital signal. Figure 3.1 illustrates a typical architecture used in A/D conversion (Clements, 1993). Although it is similar to the front-end of analog I&C systems, this architecture includes an *A/D converter*, *analog multiplexer*, and *anti-aliasing filters*. For many multi-channel systems, analog multiplexers select an analog channel for processing. Anti-aliasing filters are analog low-pass filters that reduce the power of high

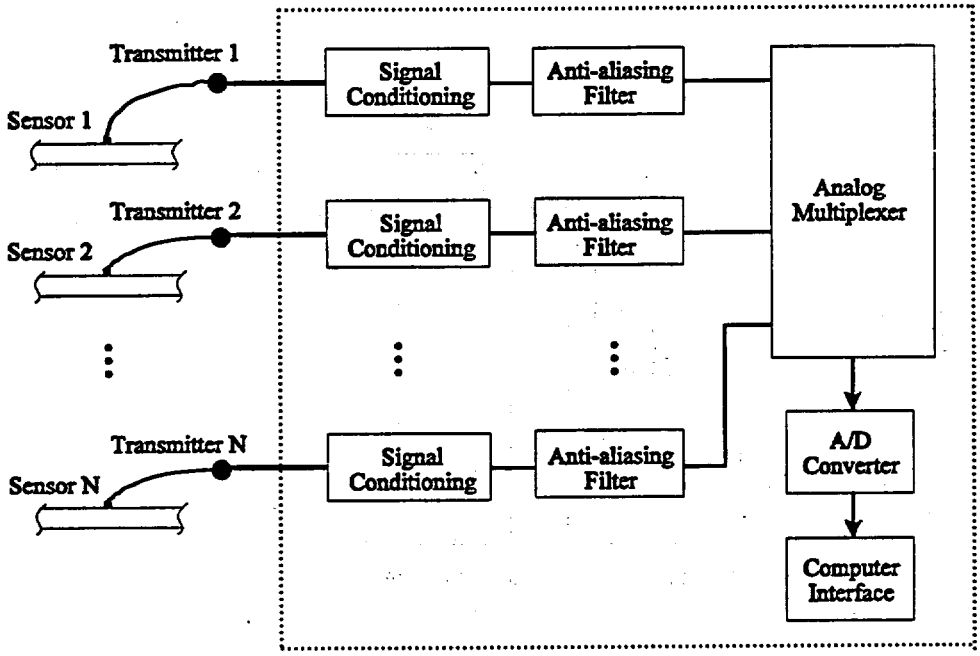


Figure 3.1 Digital I&C system front-end

frequency components in analog signals. Anti-aliasing filters and A/D converters are explained in more detail later in the chapter.

Not all digital I&C front-ends have the same architecture of Figure 3.1. For example, some transmitters include the functions of the transmitter, signal conditioner, anti-aliasing filter, and A/D converter into a single device. The output of the transmitter is a digital signal that is sent directly to the computer interface. Other architectures may include digital filtering after A/D conversion. The purpose for using a digital filter after A/D conversion is explained in Section 3.3.2.2.

Regardless of the front-end, errors enter the input signal between the plant system and computer interface. These error sources can affect the performance of protection, control, alarm, and monitoring systems in nuclear facilities. Example errors include instrument drift, nonlinearities in sensors, noise coupling in cables, and saturation effects in amplifiers. This chapter covers one particular error source, aliasing, which enters at the point of A/D conversion. To address aliasing, it is necessary to discuss A/D converters first.

3.1.1 A/D Converters

A/D conversions begin with sample requests generated by the A/D converter or an external controller. These requests are generated synchronously or asynchronously. Since the majority of applications employ a synchronous (fixed sample rate) sample request scheme, it is the only scheme considered in the report. Furthermore, it is difficult to analyze aliasing concerns in asynchronous sample rate systems.

Upon receiving a sample request, the A/D converter measures the input voltage and represents it with a binary value. Figure 3.2 illustrates the binary output of a hypothetical 3 bit A/D converter (Hoeschele, 1994). Like analog I&C systems, input

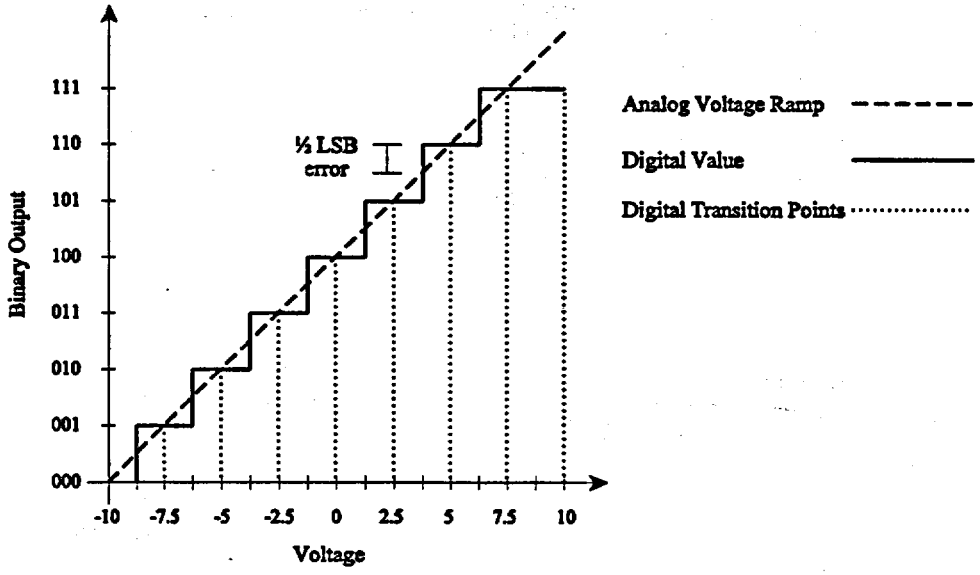


Figure 3.2 A/D transfer function

voltages for digital I&C systems are limited to a fixed range of values, as determined by external or internal circuitry. Regardless of the converter, there is a limitation to the number of bits (and thus values) to represent the analog signal sample. Typical wordlengths for A/D converters are 8, 10, 12, 14, and 16 bits. Appendix A presents the popular types of A/D converters and their operation.

For example purposes, the 3-bit A/D converter of Figure 3.2 is used to illustrate A/D converter concepts. This converter has an input voltage range of -10 to +10V and a binary output range of "000" to "111." The plot shown in Figure 3.2 is called an *A/D transfer function.* It is often used to describe A/D converter errors.

3.1.2 A/D Converter Error Sources

Understanding A/D converter errors and their impact on accuracy calculations for nuclear I&C systems is important. For instance, A/D converter errors may affect the uncertainty in setpoint calculations. The following A/D converter errors are described: *least-significant-bit (LSB) error, linearity error, gain error, offset error, non-monotonicity,* and *missing code* (Daugherty, 1995; Hoschele, 1994; National Semiconductor Corp., 1976).

LSB error: This error is present in all A/D converters. LSB represents the smallest change resolved by an *n*-bit converter, which is equal to 1 part in 2^n. Because an A/D converter cannot resolve voltage below the LSB, some amount of error exists. The maximum LSB error is ½ the LSB. For example, a 12-bit A/D converter has 0.5 part in 2^{12}, or 0.0122% of full-scale input voltage as its maximum LSB error. As an analogy to an analog error source, LSB error is similar to instrument measurement error since the actual error lies between zero and +/- some observed maximum boundary. The A/D transfer function in Figure 3.2, illustrates LSB error.

Linearity error: Linearity error, measured in LSB, describes the departure from the linear A/D transfer function curve. This type of error is similar to the nonlinear behavior experienced in many instruments. In Figure 3.3, the dashed, diagonal line illustrates the linear characteristic of the ideal A/D converter. If the steps are skewed so the line is curved instead of straight, the transfer function exhibits a linearity error.

There are two types of linearity errors: *non-linearity* and *differential nonlinearity (DNL) errors.* Nonlinearity error is the deviation between binary transitions in the actual and ideal A/D transfer functions. The specified nonlinearity error is the largest deviation for the entire transfer function. In Figure 3.3, the nonlinearity error for the A/D converter is 1½ LSB. The 1½ LSB nonlinearity error is the largest difference between the ideal and actual transfer function occurring at the "100/101" transition point.

DNL error is the amount of change going from one binary state to another for the actual A/D transfer function. To measure DNL error, the normal transition difference (1 LSB) is subtracted from the

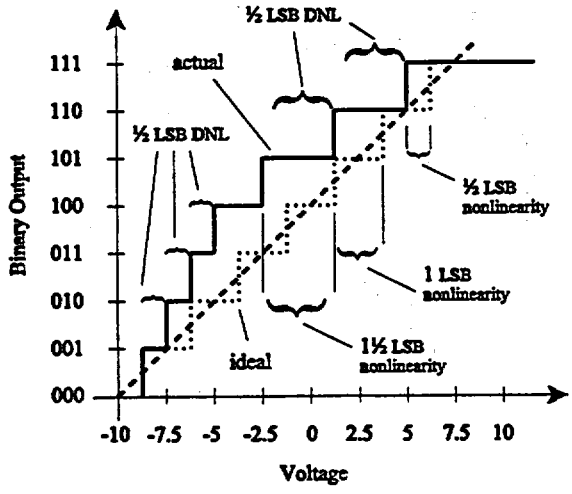


Figure 3.3 Linearity error

from the total difference. For example, in Figure 3.3, the difference between the '100/101' transition point and the '101/110' point is 1½ LSB. Accounting for the normal transition jump of 1 LSB, the remaining total, and thus the DNL error, is ½ LSB.

Gain error: Gain error, or *full-scale error*, occurs when the voltage increment is greater or less than the ideal voltage increment between transition points for all binary codes. This type of error causes the slope of the A/D transfer function to deviate from the ideal, and it is similar to the gain error that would appear in analog amplifiers. Figure 3.4 illustrates gain error.

Offset error: Offset error, or *zero error*, creates a right or left shift in the A/D transfer function. Offset errors are a result of internal converter imperfections, amplifier offsets, or ground problems. Since this error results from analog problems internal to the A/D converter, the result of offset error is similar to offset errors experienced with some analog components. With offset error, all digital transition points deviate from the ideal by the offset voltage amount.

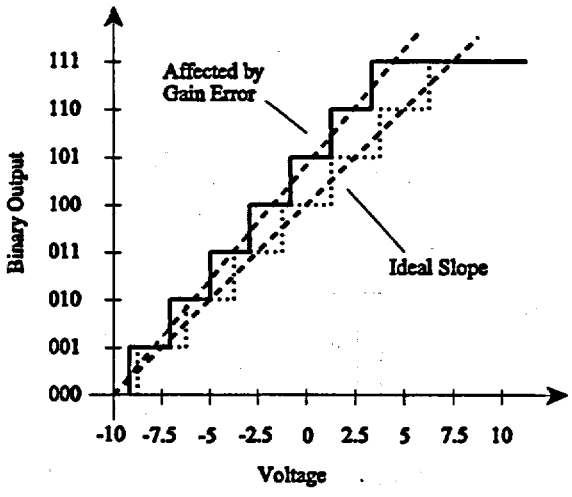


Figure 3.4 Gain error

Non-monotonicity: Non-monotonicity is the decrease in binary output for an increasing input voltage. If the DNL error is below 1 LSB, non-monotonicity is not present (unless the A/D converter has failed). Figure 3.5(a) presents an example of non-monotonicity.

Missing Code: Missing code results in one value being skipped for an increasing input voltage. Like non-monotonicity, if the DNL error is below 1 LSB, missing code is not present. Figure 3.5(b) presents an example of missing code. If non-monotonicity or missing code exist, all significant bits below the bit in error provide incorrect data.

DC1: The A/D converter's least significant bit (LSB), linearity, offset, and gain error are potential sources of signal error.

Example:

A 12-bit A/D converter has an input voltage range of 0 to 10 V. Table 3.1 provides the A/D error specifications in LSB and % full-scale of input voltage. The total A/D converter error is equal to 9 LSB, or 0.2196% of full-scale voltage. The total % full-scale voltage error multiplied by the input voltage range provides the maximum voltage error (10 V x 0.002196 = 22 mV).

Table 3.1 Example error specifications

Error	LSB	% full-scale
Least-significant bit	0.5	0.0122
Nonlinearity	2	0.0488
Differential nonlinearity	1.5	0.0366
Offset	2	0.0488
Gain	3	0.0732

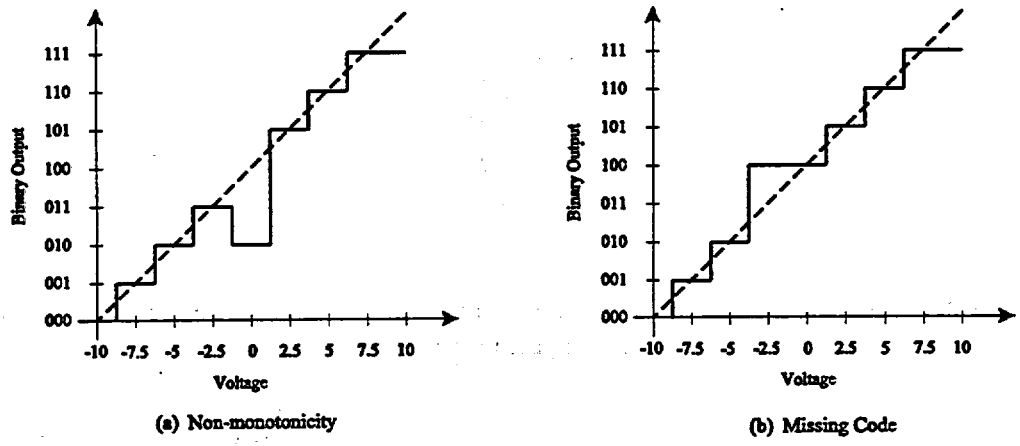


Figure 3.5 Non-monotonicity and missing code

In the example, the A/D converter errors are totaled using the algebraic method. The algebraic method is the default, conservative method for totaling errors. The other method, square-root-of-the-sum-of-the-squares (SRSS), may be used if justification is provided to show the A/D converter errors are random, independent errors with a normal distribution (ISA, 1982; USNRC, 1986).

3.2 Digital Sampling and Aliasing

Sampling is a process of translating analog signals into digital signals. From the frequency domain perspective, there is a distinct difference between analog and digital signals. It is important to understand what occurs in the frequency domain, since it clarifies the following problem. In the process of sampling, high frequencies in the analog signal may be misrepresented as low frequencies in the digital signal. This misrepresentation of frequencies is called aliasing. A theoretical principle, called *Shannon's Sampling Theorem*, stipulates a minimum sample rate to avoid aliasing. In practice, however, it is difficult to meet the assumptions for Shannon's Sampling Theorem. In practical systems, aliasing is avoided through techniques such as oversampling and the use of anti-aliasing filters. These techniques are explained later in this chapter.

3.2.1 Comparison of Analog and Digital Signals in the Frequency Domain

The effects of sampling are best seen in the frequency domain (Franklin et al., 1994; Phillips and Nagle, 1995). Figure 3.6(a) illustrates the frequency spectrum magnitude of a typical analog signal. When an analog signal is digitally sampled, only those signal frequencies below half of the sample rate (1/2T) are captured and represented in the digital signal. All frequencies above the sample rate "fold" back and add to those frequencies below 1/2T. Figure 3.6(b) illustrates this folding, or "mirroring" effect. As a result of the limited capture of signal frequencies and the folding of frequencies beyond half of the sample rate, a new frequency spectrum magnitude is created. This frequency spectrum is the frequency spectrum of the digital signal as shown in Figure 3.6(c).

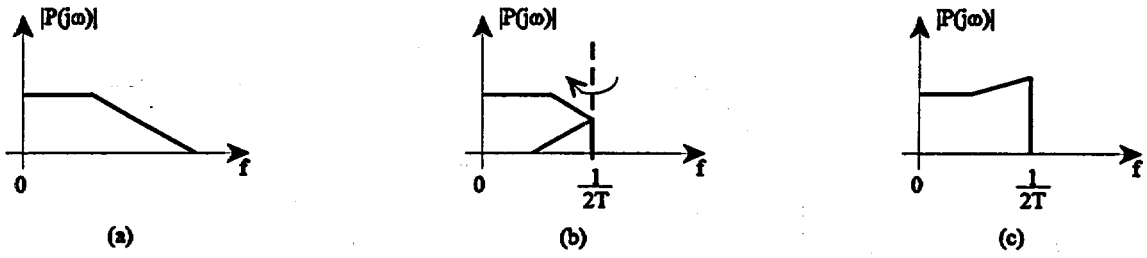


Figure 3.6 Frequency spectrums representing: (a) an analog signal, (b) frequency folding, and (c) an aliased digital signal

3.2.2 Aliasing

The difference between the analog and digital frequency spectrums shown in Figure 3.6 is the result of *aliasing*. As mentioned earlier, aliasing is the misrepresentation of signal frequencies. In particular, the signal frequencies above half the sample rate are misrepresented as frequencies below half the sample rate because of the frequency folding. These aliased frequencies add to the frequencies below half the sample rate and create a new frequency spectrum. In Figure 3.6(b), half of the sample frequency, 1/2T, is the point at which frequency folding, or aliasing occurs. It is commonly known as the *Nyquist frequency* (Nyquist, 1928). If there are any frequencies in the analog signal above the Nyquist frequency, they are aliased (Ludeman, 1986).

There is a potential for aliasing anytime digital sampling is incorporated. The only way to avoid aliasing is to set the sample rate so that all the signal frequencies are below the Nyquist frequency. This idea is summed up in *Shannon's Sampling Theorem.*

3.2.3 Shannon's Sampling Theorem

In 1949, Claude Shannon published a theorem addressing aliasing (Shannon, 1949). The following is Shannon's Sampling Theorem:

> Consider a continuous-time signal p(t) with the highest frequency component f_o Hertz, and assume that this is sampled at a frequency f_s Hertz. Then it is possible to reconstruct $p(t)$ from its sampled version $p^*(t)$ if, and only if, $f_s > 2f_o$.

Shannon's Sampling Theorem simply states that, in order to avoid aliasing, the sample frequency must be two times faster than the highest frequency in the signal. Although Shannon developed the theorem, it is sometimes called Nyquist's Sampling Theorem. Appendix B presents a theoretical derivation of Shannon's Sampling Theorem.

3.2.4 Practical Considerations

Shannon's Sampling Theorem assumes two ideal conditions. First, it assumes the A/D converter takes the sample instantaneously. In practice, it takes some time for the A/D converter to sample (usually on the order of nanoseconds). However, with sample-and-hold devices and faster sampling speeds, the A/D converter delay does not come into play for many commercial nuclear applications.

A big assumption with Shannon's Sampling Theorem is a *band-limited signal* (Smith, 1998). A

band-limited signal does not have frequency components above a particular frequency. In practice, most signals are not band-limited. Electrical noise and plant processes contribute high frequency components well above the frequencies of interest in a signal. Without an extremely high sample rate (practically infinite sample rate), aliasing occurs. With practical, digital I&C systems, some level of aliasing is always present.

3.2.5 Aliasing Prevention Techniques

Since aliasing is not eliminated in real-world systems, it needs to be controlled. As an error source, aliasing should be considered in uncertainty calculations for digital safety-related systems. One way to address aliasing is to sample the analog signal extremely fast, in which case aliasing still occurs, but the power of aliased frequencies is extremely low. Another approach is to attenuate, or reduce the power of, unwanted high frequencies before sampling by using analog low-pass filters. Both of these aliasing prevention techniques are addressed in the next section.

3.3 Sample Rate Selection Techniques

Several techniques exist for sample rate selection. This section introduces sample rate selection techniques with the goal of meeting safety, performance, and reliability criteria for digital I&C systems. Example criteria include minimizing aliasing error, meeting response-time requirements, and achieving control system stability margins. This section breaks down the different types of I&C systems along with sample rate selection techniques suitable for those types of systems. The goal is to realize the assumptions, procedures, and precautions for the various sample rate selection techniques.

Sample rate selection is dependent upon the input signal properties. For safety systems, it is important to obtain frequency information on the worst-case transients for sample rate selection. The worst-case transients represent the sharpest changes that would be experienced from plant variables. As a result of the sharp changes, the worst-case transients contain the largest amount of high frequency information the plant variable can express. When selecting a sample rate, it is important to capture the high frequency information related to the plant variable, but reject the high frequencies that arise from process and electrical noise. For this reason, it is best to use the frequency spectrums of the worst-case transients in the sample rate selection process. Techniques for obtaining the frequency spectrum of a signal are provided in Appendix D.

Nuclear I&C systems are categorized into two groups: discrete and continuous. *Discrete I&C systems* are those systems monitoring "on/off" analog signals. Sources of "on/off" signals are relays and bistables. *Continuous I&C systems* are those systems whose input signals take on a range of values. Examples are neutron monitoring and feedwater control. Continuous I&C systems are further grouped as *open-loop* and *closed-loop I&C systems*. Open-loop I&C systems generally cover protection, monitoring, alarm, and open-loop control systems. The majority of closed-loop I&C systems are those involving closed-loop control. Figure 3.7 illustrates the types of nuclear I&C systems.

3.3.1 Discrete I&C Systems

Discrete signals are those output signals from relays, bistables, etc., taking on one of two discrete voltage values. In discrete applications, the digital I&C system polls an output device to detect its state. Since there are only two discrete states, it is difficult to produce aliasing errors. Therefore, aliasing is not a concern for discrete I&C systems.

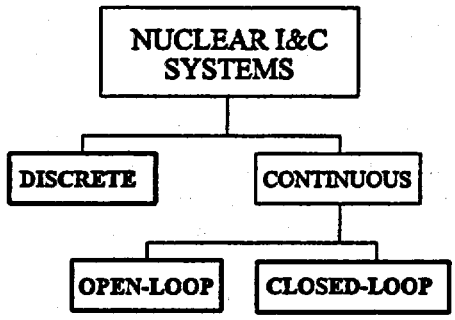


Figure 3.7 Types of nuclear I&C systems

Although aliasing is not a problem, response-time requirements affect sample rate selection for discrete I&C systems (as well as continuous I&C systems). When evaluating response-time requirements, the worst-case delay for sampling effects (time interval between samples) and the worst-case transient for the nuclear system provide the most conservative sample rate selection. This approach ensures the I&C system is capable of meeting all postulated events.

DC2: Sample rate selection is influenced by response-time requirements of the digital system.

3.3.2 Open-loop I&C Systems

In open-loop I&C systems, analog signals are sampled and used in protection, monitoring, alarm, and control functions. Example applications are reactor protection, data recording, and radiation alarms. The analog input signal takes on a range of values and accuracy requirements are often placed on these types of applications.

Sample rate selection for open-loop I&C systems are affected by accuracy and response-time requirements. Although there may be other methods for sample rate selection, two methods are presented here. These are the *oversampling* and *sampling ratio methods*. A third method, the *rise-time method*, is presented in Section 3.3.3 and may be applicable to open-loop systems if there are no strict accuracy requirements. Appendix E demonstrates the effect of sample rate selection on a nuclear protection channel.

DC3: Accuracy of input signals is affected by the level of aliasing.

3.3.2.1 The Sampling Ratio Method

As mentioned earlier, one way to avoid aliasing is to attenuate high frequencies that can be aliased. This is carried out with an anti-aliasing filter, which is an analog low-pass filter placed in front of the A/D converter. Appendix C describes several types of analog low-pass filters commonly used as anti-aliasing filters.

The sampling ratio method presented in this report is just one type of sample rate selection method that uses anti-aliasing filters. Other methods that use anti-aliasing filters do not necessarily follow the procedures outlined here. The advantage of the sampling ratio method is that it provides a way to meet accuracy requirements in reference to aliasing error. The sections that follow describe the requirements, assumptions, and procedure for using the sampling ratio method (Smith, 1998).

Inputs to Sample Rate Selection

Sample rate calculation using the sampling ratio method is based on the following three items:

- signal frequency spectrum,
- type of anti-aliasing filter, and
- allowable error contributed by aliasing.

The signal's *frequency spectrum* is the frequency domain view of the signal (see Appendix D). Within the frequency spectrum, the desired range of frequencies, or *signal bandwidth*, provides useful information about the plant process. Normally, the signal bandwidth contains those frequencies from zero frequency up to a specific frequency. The signal

bandwidth is denoted by the upper frequency range. Frequencies beyond the signal bandwidth contain high frequency plant process information or electrical noise. These frequencies are not useful in calculations, but could alias onto the signal bandwidth. The second input is the type of anti-aliasing filter used (see Appendix A). And, the third input, allowable aliasing error, specifies the level of aliasing tolerable to the system.

DC4: Typically, the worst-case transient frequency spectrum (including the signal bandwidth and high frequencies), the type of anti-aliasing filter, and the allowable aliasing level are inputs to the sample rate selection process for open-loop systems.

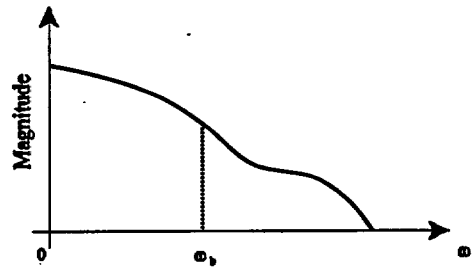
Assumptions

The sampling ratio method makes two assumptions about the frequency spectrum and anti-aliasing filter:

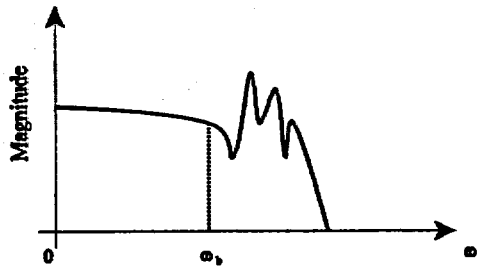
- Frequencies beyond the signal bandwidth are lower in magnitude than those within the bandwidth.
- The cutoff frequency of the anti-aliasing filter is equal to the signal bandwidth.

The first assumption requires frequencies within the signal bandwidth to be of larger magnitude than those outside the bandwidth. Figure 3.8(a) illustrates a frequency spectrum, with signal bandwidth ω_b, meeting this assumption. Some systems may not meet this assumption. For example, plant signals may suffer from a large amount of 60 Hz noise. This type of noise, as well as other electromagnetic interference/ radio-frequency interference (EMI/RFI), may cause frequencies outside the signal bandwidth to be of higher magnitude than the frequencies within the signal bandwidth (USNRC, 1994, 1996b, 1997c; EPRI, 1994). In this case, the sample rate selection is not conservative because there is no guarantee that the anti-aliasing filter will adequately attenuate unwanted high frequencies to meet aliasing error requirements. If unwanted high frequencies are lower in magnitude than those within the bandwidth, then assurance of meeting targeted allowable aliasing error level can be made. Figure 3.8(b) illustrates a frequency spectrum, in which frequencies outside the bandwidth are higher in magnitude than those within the bandwidth.

The second assumption requires the cutoff frequency of the anti-aliasing filter to equal the signal's bandwidth. This assumption provides for simple calculation of the sample rate while achieving optimum attenuation of higher frequencies.



(a) Conservative frequency spectrum



(b) Non-conservative frequency spectrum

Figure 3.8 Conservative vs. non-conservative frequency spectrum

***DC5:** When the sampling ratio method is used for sample rate selection, the following assumptions are evaluated for their validity: (1) frequencies beyond the signal bandwidth are lower in magnitude than those within the bandwidth and (2) the cutoff frequency of the anti-aliasing filter is equal to the signal bandwidth.*

Sampling Ratio

The *sampling ratio* determines the necessary sample rate to ensure the allowed aliasing error level is not surpassed. The sampling ratio (SR) is defined as:

$$SR = \frac{\text{sample rate}}{\text{max. desired bandwidth frequency}}$$

Figure 3.9 illustrates the relationship between the anti-aliasing filter frequency response, the Nyquist frequency (S/2), the allowed aliasing error level, the signal bandwidth (F_D), the folded portion of the frequency spectrum, and the frequency of required attenuation on the anti-aliasing filter (F_R). The figure relates for a given allowable aliasing error, the minimum Nyquist frequency to meet the aliasing error specification.

Looking at Figure 3.9, the Nyquist frequency is the average value of the signal bandwidth and the frequency of required attenuation,

$$\frac{S}{2} = \frac{F_D + F_R}{2}$$

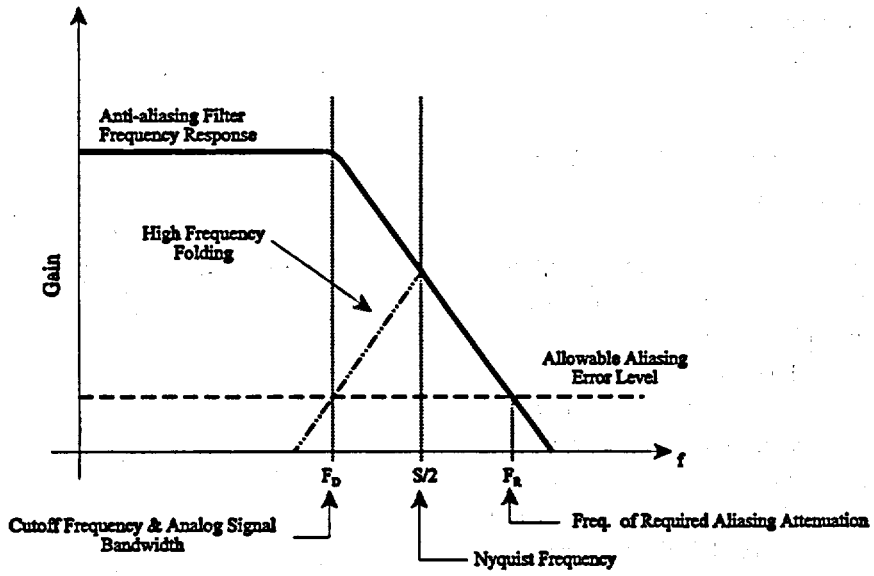


Figure 3.9 Allowable aliasing level, anti-aliasing filter, and sample rate relationship
Source: Technology Training Institute, Santa Barbara, California

The sampling rate is then equal to

$$S = F_D + F_R$$

and the sampling ratio equates to

$$\frac{S}{F_D} = 1 + \frac{F_R}{F_D}$$

It is important to understand several principles of the sampling ratio method. First, the lowest possible sampling ratio is 2, agreeing with Shannon's Sampling Theorem. Second, by placing the cutoff frequency of the anti-aliasing filter equal to the signal bandwidth, frequencies within the signal bandwidth are kept at the same magnitude, while unwanted high frequencies are attenuated.

Notice in Figure 3.9 that the anti-aliasing filter's frequency response is used to illustrate the sample rate, rather than the signal's frequency spectrum. For one, working with the filter's frequency response is easier than using the frequency spectrum. However, a more important reason for using the anti-aliasing filter's frequency response is design conservatism. Consider a worst-case frequency spectrum (allowed by the method's assumptions) as one having the same magnitude for all frequencies extending to infinity. It is desirable to sample this signal and capture frequency information up to a particular bandwidth. If the anti-aliasing filter's cutoff frequency is set equal to the signal's bandwidth, then the signal's frequency spectrum, after filtering, looks like the anti-aliasing filter's frequency response. When sampling occurs, frequencies above the Nyquist frequency fold onto the lower frequencies as illustrated in Figure 3.9. In this worst case, the allowable aliasing error requirement is met. Normally, frequencies outside the signal bandwidth are smaller in magnitude than those within the bandwidth. When sampling occurs, these high frequencies fold onto the lower frequencies with less aliasing affect than the worst-case signal just described.

With the sampling ratio equation it is possible to calculate the sampling ratio for any anti-aliasing filter. The sample rate is found by multiplying the sampling ratio by the signal's bandwidth. Table 3.2 presents the sampling ratios for various filters and allowable aliasing error.

Example

A recorder logs data from a pressure signal. The following data are gathered for sample rate selection:

- Signal bandwidth — 10 Hz
- Anti-aliasing filter — RC passive filter
- Allowable aliasing error — 1% of actual value
- Assumptions for the sampling ratio method met

With F_D equal to 10 Hz and the sampling ratio equal to 101 (from Table 3.2), the required sample rate is 10 x 101, or approximately 1 kHz. The sample period is equal to 1/sample rate or, in this case, 1 msec.

DC6: Sample rate selection calculations describe how the chosen sample rate and anti-aliasing filter meet the allowable aliasing requirements.

3.3.2.2 The Oversampling Method

Oversampling limits aliasing problems by sampling extremely fast. One particular type of A/D converter, the Sigma-Delta converter, samples at rates into the megahertz range (see Appendix A). By sampling very fast, it is assumed that signal frequencies above the Nyquist frequency have very low power. When these high frequencies are aliased, they do not cause significant signal corruption because of their low power. The requirements for the sampling ratio method are the same for the oversampling method. Often, anti-aliasing filters are used in combination with the oversampling method. Although there is no outlined method for selecting the sample rate or anti-aliasing filter, the combination is arranged so the allowable aliasing margins are met.

Table 3.2 Sampling ratios for different anti-aliasing filters

Allowable Aliasing Error	1% (-40dB)	0.1% (-60dB)	0.01% (-80dB)
RC-filter	101	1001	10001
2-pole Bessel	13.4	41	128
2-pole Butterworth	11	33	101
4-pole Bessel	5.7	9.5	16
4-pole Butterworth	4.1	6.7	10.9
6-pole Bessel	4.6	6.5	9
6-pole Butterworth	3.2	4	5.6
8-pole Bessel	4.4	5.5	7.1
8-pole Butterworth	2.8	3.4	4.1
8-pole/8-zero Elliptical	2.2	2.3	2.4

Source: Technology Training Institute, Santa Barbara, California

Example

A pressure signal, with an allowable aliasing error requirement of 1%, is sampled using the oversampling technique. In this case, high frequencies within the pressure signal do not change for normal and abnormal operation (may or may not be the case for other systems). Therefore, the designer obtains the frequency spectrum of the pressure signal at normal operation. He plans to sample at 1 MHz, giving a Nyquist frequency of 500 kHz. Looking at the frequency spectrum, the magnitude at 500 kHz is -67 dB, and the magnitude of frequencies above 500 kHz is less than -67 dB. Since the allowable aliasing error level is 1%, or -40 dB, when those frequencies beyond 500 kHz fold, they will contribute less than -67 dB of aliasing error, thus meeting the aliasing requirement.

DC7: When the oversampling method is used, the sample rate is sufficiently high enough that resulting aliasing is below allowable requirements.

Oversampling is a simple way to address aliasing; however, two precautions should be evaluated. First, the designer should be aware of the amount of data. Because of high sample rates, a significant amount of data is produced. Data are reduced by first filtering the sampled data with a digital filter, and then taking every n^{th} data point and throwing away the rest (decimation). It is important to filter the data first, then decimate, to avoid aliasing of the sampled data. Second, designer must ensure that downstream data processing is capable of handling the characteristic of the data. For example, some older analog I&C systems used large analog filters to remove signal noise before data processing. If that system is replaced by an oversampling digital I&C system, the data coming from the new digital I&C system may contain high frequencies for which downstream data processing may not handle.

DC8: When the oversampling method is used, it may capture a large amount of high frequencies that could negatively affect downstream plant equipment.

Although oversampling is meant to avoid aliasing problems, there is still a precaution that significant aliasing may occur. For instance, it is often assumed that sampling ten times faster than the signal bandwidth alleviates aliasing problems. In this case, a digital filter is often used after sampling to remove signal noise captured by oversampling. Figure 3.10 illustrates a digital filter used in this capacity.

By using the digital filter it is often thought that any aliasing that may have occurred is now removed. However, there is still a potential for significant aliasing error. When an analog signal is sampled, frequencies above the Nyquist frequency fold on top of lower frequencies. A digital filter attenuates frequencies beyond its cutoff frequency, but it cannot remove those aliased frequencies within the filter's bandwidth. Since, digital filters cannot remove aliased frequencies that fall within its bandwidth, it is better to use an anti-aliasing filter to meet aliasing requirements. Even with the Sigma-Delta converter, which samples into the megahertz range, a simple RC filter is recommended as an anti-aliasing filter (Pang, 1998).

3.3.3 Closed-loop I&C Systems

Until now, sample rate selection has focused on open-loop I&C systems. Now, the focus centers on sample rate selection for closed-loop I&C systems. The most common type of closed-loop system in

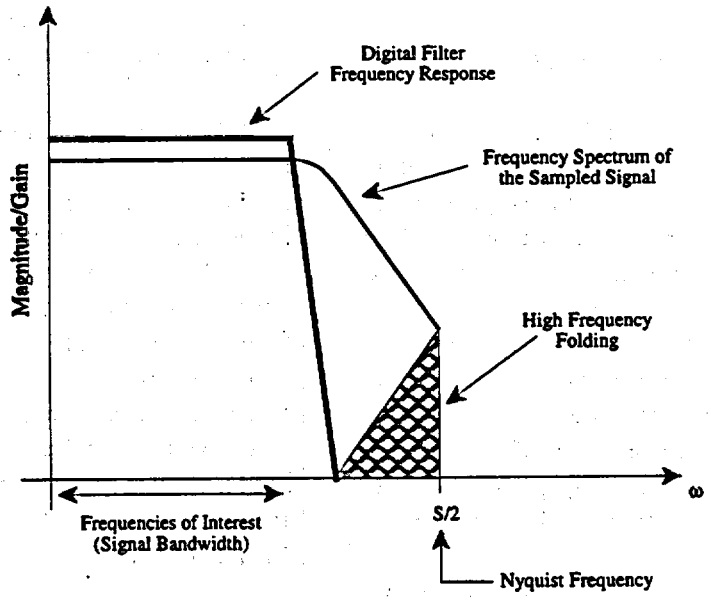


Figure 3.10 Use of a digital filter after sampling

nuclear facilities is closed-loop control. In closed-loop control systems, the feedback signal bandwidth is the bandwidth of the closed-loop control system. Therefore, the theoretical minimum sample rate is twice the bandwidth of the closed-loop control system (Houpis and Lamont, 1992). Sample rates below the minimum sample rate may cause instability or unpredicted behavior. Appendix F demonstrates the effects of sampling on a digital control system.

The following three sample rate selection methods for closed-loop control are described:

- phase/gain margin method,
- closed-loop bandwidth method, and
- signal rise-time method.

The primary concern in sample rate selection for closed-loop control is instability. However, aliased noise may have the potential to upset these systems. Where high levels of noise exist in reference or feedback signals or where accuracy requirements are placed on such signals, refer to the open-loop I&C system section for guidance.

3.3.3.1 Phase/Gain Margin Method

If a mathematical model for the closed-loop control system exists, a simple way to ensure stability is through the *phase/gain margin* of the digital control system. Determining the phase/gain margin of a digital control system is found in several digital control texts (Phillips and Nagle, 1995; Franklin et al., 1994). Using the control system's open-loop frequency response, the gain margin is the amount of gain added to the controller before instability occurs. Phase margin is the amount of phase added before instability occurs. Digital sampling adds delay (phase) to closed-loop control systems, reducing their phase margin.

In the phase/gain margin method, the open-loop frequency response of the digital control system is observed. It is important to use the frequency response of the digital control system since the analog control system has more phase margin. If the phase/gain margin meets the control system requirements, then the sample rate is sufficient for stability.

DC9: The adequacy of sample rates in closed-loop digital control systems may be determined by the phase/gain margin.

3.3.3.2 Closed-loop Bandwidth Method

If a control system does not have phase/gain margin requirements, an easier method for sample rate selection is through the closed-loop bandwidth. Although sample rates greater than twice the closed-loop bandwidth should provide stability, it is often suggested to sample at least six times faster than the bandwidth (Franklin et al., 1994). Increasing the sample frequency causes the digital control system response to approach that of a corresponding analog control system.

DC10: If the closed-loop bandwidth method is used, the sample rate selection in closed-loop control systems, the sample rate is typically six times higher than the closed-loop bandwidth.

3.3.3.3 Signal Rise-time Method

In the process control industry, a rule of thumb is often used to calculate the sample rate for a system. This rule of thumb states that the sample rate should be chosen so that the signal of concern is sampled 4 to 10 times on its rising edge (Astrom and Wittenmark, 1997). The rising edge, or rise time, is defined as the time it takes a variable to rise from 10% of its final value to 90% of its final value (Nise, 1992; Westphal, 1995). Astrom and Wittenmark relate sample rate to the rise time of an analog control system response. Their equation

$$N_r = \frac{T_r}{h}$$

uses the number of samples per rise time, N_r, the rise time, T_r, and the sample period, h. The idea is to arbitrarily pick N_r between 4 and 10. Knowing the rise time, the sample period (and thus, the sample rate) is calculated.

To test the rule of thumb, consider the first-order lag step response, having the following transfer function:

$$\frac{1}{s+1}$$

Figure 3.11 illustrates the first-order lag response to a step input. To sample the signal 4 times on the rising edge (from 10 to 90% of the final value), with the rise time approximately equal to 2 seconds, requires a sample period of 0.5 second, or a sample rate of 2 Hz. Looking at the frequency response of the first-order lag, the bandwidth is 1 radian/sec, or 0.16 Hertz. Using Shannon's Sampling Theorem, the theoretical minimum sample rate is 0.32 Hertz. The rule of thumb provides a sample rate 6.25 times faster than the bandwidth of the first-order lag in this particular case.

***DC11:** If the rise-time method is used for sample rate selection in closed-loop systems, the number of samples per rise time is typically greater than or equal to four.*

The rise-time method has the advantage of easily calculating the sample rate from time responses and open-loop frequency responses. In addition, it can be used with open-loop I&C systems. In this capacity, it has two disadvantages:

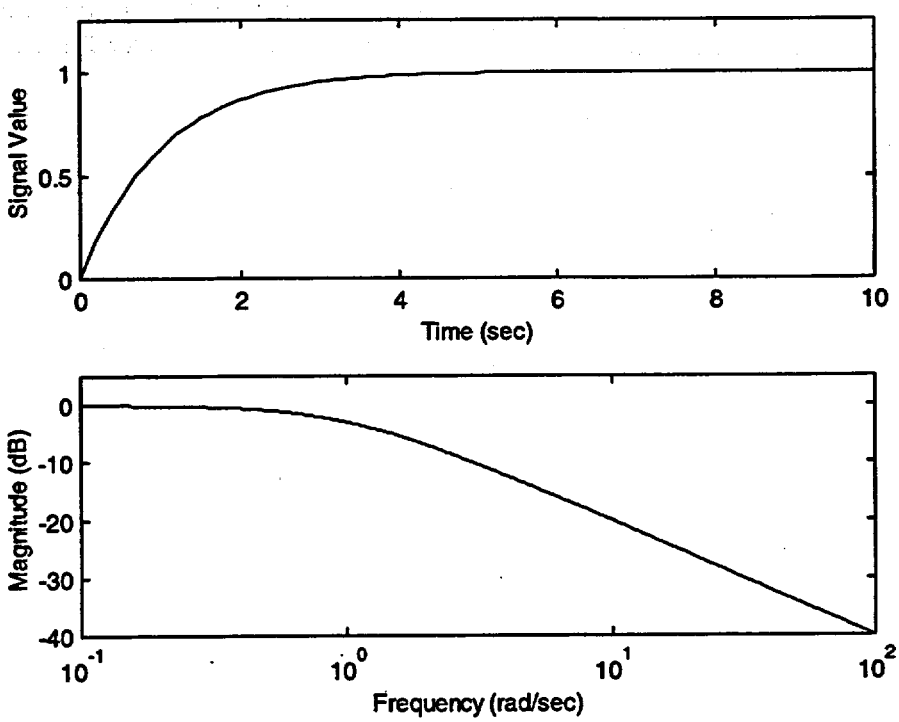


Figure 3.11 Time and frequency response for a first-order lag

- It does not take into account noise that could be aliased.
- It does not readily justify allowable aliasing error compliance.

For safety systems, sample rate selection is better carried out using one of the methods described in the open-loop I&C application section. The rise-time method is suitable for systems that do not have accuracy requirements and for control systems for which there are no mathematical models.

3.4 Summary

Sample rate selection is important to accuracy, response-time, and stability requirements in digital I&C systems. Aliasing is a type of error appearing in digital sampling applications to some degree. Aliasing folds frequencies above the Nyquist frequency on top of those frequencies below. This folding of frequencies alters the frequency spectrum and creates an error between the analog signal and its digital representation.

The sample rate selection method depends upon the type of digital I&C system. If the system handles discrete signals, there are no aliasing concerns; however, there may be response-time concerns. Sample rate selection for open-loop systems can be performed using the sampling ratio method, the oversampling method, or a combination of the two. The goal in open-loop systems is to keep aliasing error below a targeted level. For closed-loop systems, sample rate is determined from the phase/gain margin method, the closed-loop bandwidth method, or the rise-time method. Improper sample rate selection in closed-loop control systems causes unnecessary plant system oscillations. The rise-time method could also be used for open-loop systems where accuracy requirements are relaxed.

In addition to aliasing concerns, A/D converter errors corrupt input signals. A/D converter errors include LSB error, linearity error, gain error, offset error, non-monotonicity, and missing code. These errors, along with aliasing errors, may impact uncertainty calculations for digital safety systems.

4 COMPUTER WORDLENGTH SELECTION

In digital instrumentation and control (I&C) systems, values are represented by a finite number of bits, called the *wordlength*. Popular wordlengths for computers are 8, 16, and 32 bits. Because of finite wordlengths, a variable can only take on a limited number of values. Table 4.1 shows the number of possible discrete values for a given wordlength size. The size of the wordlength is determined by the digital system hardware (i.e., computer bus, processor). Because of finite wordlengths, the accuracy of the digital I&C system is limited (Williamson, 1991). Finite wordlengths affect all signals within the digital I&C system as well as algorithm coefficients (Franklin et al., 1994). This chapter describes the effects of finite wordlengths on digital I&C performance, and the design techniques to avoid or minimize these effects.

Table 4.1 Wordlengths and corresponding number of discrete values

Wordlength	Number of Possible Discrete Values
8 bit	256
16 bit	65,536
32 bit	4,294,967,296

4.1 Finite Wordlength Effects on Input Signals

Because of finite wordlengths, errors exist between the true analog value and the sampled value. A/D converter resolution describes the minimum amount of error existing in the binary output. The following equation describes A/D resolution (Clements, 1993):

$$\text{Resolution} = (\text{A/D Range})/(2^n - 1),$$

where n is the number of bits. Table 4.2 presents the resolution for various A/D wordlengths. To reduce the error attributed to A/D resolution, choose A/D converters with larger wordlengths. Resolution is similar to least significant bit (LSB) error mentioned in Section 3.1.2.

Table 4.2 A/D resolution for various wordlengths

Wordlength	Resolution (% of full scale)
8 bit	0.392160
10 bit	0.097752
12 bit	0.024420
14 bit	0.006104
15 bit	0.003052
16 bit	0.001526
18 bit	0.000381
20 bit	0.000095
22 bit	0.000024

Dynamic range (DR) is a concept associated with A/D resolution. Dynamic range is the ability to observe small changes over wide input ranges (Razavi, 1995). The formula for calculating DR is

$$DR = \frac{\text{Full - scale Value}}{\text{Smallest Reliable Sensed Value}}$$

The smallest reliable sensed value is determined by the A/D errors and resolution. For example, if a 20-bit A/D converter has an input voltage range of 0 to 10 V, the resolution is calculated by the following:

$$10V/(2^{20} - 1) = 9.5\mu V$$

and the dynamic range is

$$10V/9.5\mu V = 1{,}052{,}631 \text{ (or 120.4 dB)}$$

However, with 3 LSB of A/D error, the smallest reliable sensed value becomes

$$9.5\mu V \times 2^3 = 76.3\ \mu V$$

This results in a dynamic range of 131,061 (102 dB). If high dynamic range is required, an A/D with a larger wordlength is required, along with low A/D converter error. If lower dynamic range is allowable, smaller wordlength A/Ds may be used.

In some applications, *headroom* may be a concern (Smith, 1998). Headroom is the ability of the A/D converter to represent analog values beyond the normal operating range. The larger the headroom, the greater the capability of the A/D converter to represent analog values beyond the normal operating range. With increasing headroom, the dynamic range of the A/D converter also increases.

DC12: Dynamic range and headroom are two computer wordlength considerations when A/D converters are specified.

4.2 Finite Wordlength Effects on Intermediate Signals

Intermediate signals are those digital signals within the computer used to calculate the results. Since registers and memory have finite wordlength, errors enter intermediate signals. Many of these errors are dependent upon the type of arithmetic notation used.

4.2.1 Fixed-point Arithmetic

There are two ways to represent values in computers: fixed-point arithmetic and floating-point arithmetic. Fixed-point arithmetic, which assumes the decimal remains in a fixed position, is simple and commonly used in digital I&C systems. Although there is no standard way of implementing fixed-point arithmetic, the following provides a general description. For example, an 8-bit computer might represent fixed-point values in the following manner:

s.mmmmmmm

where *s* is the sign bit and *m* is a binary place value. In this implementation, the decimal place is after the sign bit. Values are represented with the decimal place to the extreme left, causing multiplication results to be smaller, and not larger, than any one of the operands.

In fixed-point multiplication, two numbers from separate registers are multiplied, creating a result that occupies the space of two registers. If values are stored using one register, it is necessary to reduce that result to fit one register. To do this, the least significant portion of the result is truncated or rounded-off, reducing the accuracy of the result.

Fixed-point addition causes round-off and truncation error when register *overflow* occurs. Overflow occurs when the addition of two numbers creates a result 1 bit larger than the register wordlength. For example, adding the following two binary numbers gives an overflow, which needs to be accounted for since it is the most significant bit:

```
      101
    + 100
overflow -> 1 001
```

Ignoring overflow conditions causes spikes on the output of a digital I&C system. These spikes are called *overflow noise*. Overflow noise is preventable and is normally identified in system tests.

In addition to the problems noted above, round-off/truncation causes the following phenomenon to occur in digital feedback control. The goal of digital feedback control is to minimize the error between a desired value and the actual value. Because of round-off and truncation, the controller cannot match the actual value to the desired value. Instead, the actual value oscillates around the desired value. Depending upon the application and the characteristics of the oscillations, this phenomenon may be of concern. These oscillations are minimized by

- Scaling the input to a level that avoids overflow while maintaining the necessary dynamic range and
- Implementing algorithms in a manner that minimizes the effects of round-off and truncation.

4.2.2 Floating-point Arithmetic

Floating-point arithmetic provides scaling of large numbers, which is difficult in fixed-point arithmetic. In the floating-point system, real numbers are represented with a magnitude and sign (mantissa) in one part of a register and the exponent in another part of the register. The floating-point representation moves the decimal point from its current place to the front of the most significant bit. When moving the decimal, the exponential portion of the number is adjusted. This type of numbering system is often called scientific notation.

Although not everyone uses it, there exists a standard for implementing floating-point arithmetic. IEEE Std. 754-1985, "IEEE Standard for Binary Floating-Point Arithmetic," presents two standard methods to implement floating-point arithmetic (IEEE, 1985). The single-precision (32 bit) IEEE floating-point representation is laid out as

s eeeeeeee mmmmmmm mmmmmmmmmmmmmmmmm

There are 8 bits in the exponent field (denoted by "e") and 23 bits for the mantissa (denoted by "m"). In the IEEE standard, a "1" is always to the left of the decimal point. For example, in the single precision format, the mantissa value would look like

1.mmmmmmmmmmmmmmmmmmmmmmm

even though the "1" is not part of the stored value. The "1" is called the hidden bit in the IEEE floating point standard. Since the mantissa has a total of 24 bits (including the hidden bit), the magnitude of the relative error is bounded by $2^{-24} = 5.96... \times 10^{-8}$. This means there is at least 7 decimal digit precision. The largest possible mantissa is $M = 2^{24} = 16777216$, which has 7+ digits of precision.

IEEE 754 also specifies a double-precision (64 bit) IEEE floating-point representation. It is laid out in the same manner as the single-precision format except for 11 bits in the exponent field and 52 bits in the mantissa field. Since the mantissa has 53 bits (counting the hidden bit), the magnitude of the relative error is bounded by $2^{-53} = 1.11... \times 10^{-16}$. This results in at least 15 decimal digit precision. The largest possible mantissa is $M = 2^{53} = 9.007... \times 10^{15}$, which has 15+ digits of precision.

While high precision is obtainable by floating-point arithmetic, but there are two precautions. First, floating-point arithmetic can suffer from truncation and round-off errors like fixed-point arithmetic, particularly if there is a large magnitude difference between two operands. These errors become more apparent as the number of bits for storing the mantissa decreases.

A second precaution involves the conversion between floating-point and fixed-point arithmetic.

COMPUTER WORDLENGTH SELECTION

Several computer-related disasters are related to the conversion problem , two of which involve the Patriot Anti-missile System and the Ariane 5 Launcher (GAO, 1992; Lions, 1996).

In the Patriot missile case, time is kept as a fixed-point number and then converted to a floating-point number for missile navigation purposes. Because the registers in the Patriot missile are limited to 24 bits, the conversion from a fixed-point to a floating-point number cannot be more precise than 2^{-24}. As the accounted time value becomes larger, the accuracy of that time diminishes. As a result of the time inaccuracy caused by the conversion, a Patriot missile battery could not intercept a Scud missile that killed 28 American soldiers.

In the Ariane 5 case, horizontal velocity is represented as a 64-bit floating-point number and converted to a 16-bit fixed-point number. In the Ariane 5's maiden flight, the horizontal velocity became too large to be converted to a fixed-point number. As a result, an operand error occurred, which shut down a dual-redundant computer sending critical data to the flight computer. Without the critical data, the flight computer caused the launcher to veer sharply from its course, break apart, and then self-destruct.

DC13: Overflow, round-off/truncation, resolution, and type/size conversion of fixed- and floating-point numbers are potential sources of computer wordlength errors.

4.3 Finite Wordlength Effects on Output Signals

Often, digital results are converted into analog signals using D/A converters. The D/A converter holds the last received value at a representative DC voltage until the next binary value arrives. At that time, it holds the new value and repeats the process. Figure 4.1 illustrates the output of a D/A converter. As shown in the figure, the output signal has a step-like nature. The resolution of the analog output signal is controlled by the update interval, ΔT, and the resolution of the D/A converter. Many actuators in nuclear facilities can handle the step-like output signal. However, some components, like hydraulic actuators, are not able to handle large steps changes (Franklin et al., 1994). In this case, the resolution of the analog output signal may be increased by shortening the update interval, or increasing the wordlength of the

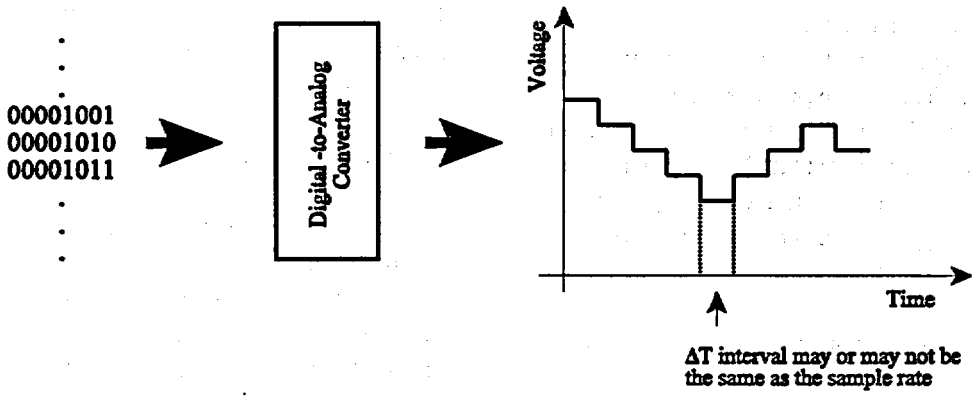


Figure 4.1 Digital-to-analog conversion

D/A converter. The output can also be smoothed by an analog low-pass filter.

DC14: Compatibility of analog output signals with downstream electrical/electronics systems are a consideration with D/A converter selection and installation. Areas of compatibility include signal shape, rate of change, range, and power level.

4.4 Finite Wordlength Effects on Coefficients

Algorithm coefficients are also affected by finite wordlengths. When developing algorithms, the real number representation is used in design evaluation. In the actual digital I&C system, coefficients are stored in memory locations having finite wordlength. The value stored in the digital I&C system may not be the same as the designed value, resulting in potential unexpected behavior (Phillips and Nagle, 1995).

There are two ways to combat coefficient round-off/truncation. First, developers may consider using the wordlength-limited coefficients in the design evaluation phase. For example, a developer normally simulates a digital filter or controller before implementing it in the actual system. In the simulation, exact coefficient values are used, but, at the time of implementation, the actual equipment limits the degree of coefficient accuracy. To account for finite wordlength limitations in coefficients, developers use the wordlength-limited version of the coefficients in the simulations.

A second way to combat finite wordlength effects on coefficients is through algorithm implementation. The sensitivity of polynomial roots increases with the order of polynomials. Slight changes in coefficients may cause a large change in polynomial roots. If algorithms are implemented as large-order polynomials, then any coefficient alteration due to finite wordlength limitations may have a large effect. If polynomials are broken into smaller polynomials, then there is less sensitivity to coefficient changes. Therefore, digital filters (and control algorithms) are typically implemented as a series of small polynomials rather than one large polynomial (Phillips and Nagle, 1995; Franklin et al., 1994).

DC15: Finite wordlength effects on algorithm coefficients may affect the accuracy of computer calculations.

4.5 Summary

Finite wordlengths introduce errors into digital I&C systems through overflow, truncation/round-off, and inappropriate type/size conversion of values. Finite wordlength errors are present in all digital I&C systems to some degree. By incorporating the proper design methods, these errors are minimized to the point at which they do not appreciably affect system operation.

Fortunately, problems related to finite wordlength effects can be detected with proper system tests which have good test coverage. For digital I&C equipment having previous operation history, finite wordlength problems are likely to have surfaced in that history.

5 SUMMARY

Several operational differences exist between analog and digital I&C systems. One operational difference is the conversion of analog signals to binary numbers by digital I&C systems. Since digital I&C systems manipulate binary numbers, they must convert analog signals to binary numbers, and in some cases, convert binary results back to analog signals. In reference to analog-to-digital conversion, two key factors are important to the performance, reliability, and safety of digital I&C systems. One factor is the sample rate, and the other factor is the computer wordlength. Sample rate and computer wordlengths are not a factor of consideration in analog I&C systems.

Problems may arise in digital I&C systems when analog signals are not sampled fast enough. When a digital I&C system samples, it gets a snapshot of the analog signal at discrete time intervals. If the signal changes rapidly and the sample time intervals are not small enough, the sampled version of the signal will misrepresent high frequency components of the original signal as low frequency components. This type of signal corruption is called aliasing.

Due to finite wordlengths, mathematical operations such as addition and multiplication introduce round-off and/or truncation errors. If finite wordlength errors are not properly addressed in digital I&C systems, they may cause unexpected behavior.

The problems mentioned above are potential hazards for nuclear I&C systems. In control systems, aliasing or severe finite wordlength errors may cause instability. In monitoring, alarm, and protection systems, such conditions may degrade performance. For protection systems in particular, aliasing and finite wordlength errors may impact setpoint accuracy and response-time requirements. However, through proper sample rate and computer wordlength selection, these error sources can be minimized to a point in which they have an insignificant effect on the system.

Sample rate selection for a particular signal depends upon its rate of change (frequency content of the signal). Shannon's Sampling Theorem states that a signal must be sampled two times faster than the signal's highest frequency component to reconstruct the signal in the time domain. This theorem defines a theoretical minimum sample rate to prevent aliasing. When practical issues, such as signal noise, are considered, the sample frequency is greater than two times the highest frequency of the analog signal. Calculation of the minimum sample rate depends upon the following:

1. Application — control, monitoring, protection, or indication

2. Environment — signal noise

3. I&C equipment — input signal filters, A/D converters, and other interfacing computer equipment

4. Interfacing systems — actuators and dynamics of the plant process

Sample rate selection methods vary, depending upon the type of digital I&C system. Types of systems include discrete, open-loop, and closed-loop I&C systems. Discrete I&C systems deal with input signals taking on one of two values, and the input signals often come from discrete devices such as relays, bistables, etc. Discrete I&C systems do not have aliasing problems, but the selected sample rate may be influenced by response-time requirements.

Open-loop I&C systems do not have feedback signals and include protection, monitoring, alarm, and some control systems. Three sample rate selection methods are commonly used with open-loop I&C applications. Two of the methods, the sampling ratio method and the oversampling method, are concerned with meeting a maximum allowable aliasing level, and

they are best suited for those systems requiring signal accuracy. Procedures for applying these two methods have been identified in the document. A third method, the rise-time method, is suitable for open-loop I&C systems that do not have stringent signal accuracy requirements.

Closed-loop I&C systems have at least one feedback signal and deal mostly with closed-loop control. There are three sample rate selection methods available to closed-loop I&C systems: the phase/gain margin method, the closed-loop bandwidth method, and the rise-time method. These methods are mainly concerned with system stability, although aliasing may be a problem in these systems also.

Sample rate selection is based upon design considerations that have their bases from fundamental engineering principles. This document has identified the following design considerations that are commonly addressed during sample rate selection.

DC1: The A/D converter's least significant bit (LSB), linearity, offset, and gain error are potential sources of signal error.

DC2: Sample rate selection is influenced by response-time requirements of the digital system.

DC3: Accuracy of input signals is affected by the level of aliasing.

DC4: Typically, the worst-case transient frequency spectrum (including the signal bandwidth and high frequencies), the type of anti-aliasing filter, and the allowable aliasing level are inputs to the sample rate selection process for open-loop systems.

DC5: When the sampling ratio method is used for sample rate selection, the following assumptions are evaluated for their validity: (1) frequencies beyond the signal bandwidth are lower in magnitude than those within the bandwidth and (2) the cutoff frequency of the anti-aliasing filter is equal to the signal bandwidth.

DC6: Sample rate selection calculations describe how the chosen sample rate and anti-aliasing filter meet the allowable aliasing requirements.

DC7: When the oversampling method is used, the sample rate is sufficiently high enough that resulting aliasing is below allowable requirements.

DC8: When the oversampling method is used, it may capture a large amount of high frequencies that could affect downstream plant equipment.

DC9: The adequacy of sample rates in closed-loop control systems may be determined by the phase/gain margin.

DC10: If the closed-loop bandwidth method is used for sample rate selection in closed-loop systems, the sample rate is typically six times higher than the closed-loop bandwidth.

DC11: If the rise-time method is used for sample rate selection in closed-loop systems, the number of samples per rise time is typically greater than or equal to four.

Finite wordlength errors occur when real-number data are represented by a finite number of bits in a computer system. These errors occur at input signal acquisition, intermediate calculations, the output signal, and algorithm coefficients. For example, finite wordlength errors are introduced at A/D conversion. The accuracy of the conversion is impacted by the A/D converter's dynamic range. As the converter covers a wider range of input values and resolves to smaller voltage levels, the dynamic range increases. The dynamic range is affected by the wordlength of the A/D converter and its associated error specification.

Intermediate calculations are affected by finite wordlengths of computer memory. Errors associated with intermediate calculations include round-off/ truncation error, overflow, and incorrect type conversion. Overflow occurs during addition when the result occupies one more bit than the available storage space. Incorrect type conversions may occur when numbers are converted between two different numbering conventions (i.e., fixed- and floating-point notation).

In many applications, digital I&C systems convert digital results into analog signals. The conversion is carried out using a digital-to-analog (D/A) converter. Because the value of the digital signal is not known between updates, the D/A converter accepts a digital value and holds it at a representative DC voltage until the next update arrives. This creates a step-like analog signal that may not be acceptable to some plant systems.

Often, when algorithms are developed for digital I&C systems, real-number coefficients are used in the design. When the coefficients are placed into the digital I&C system, truncation or round-off of the coefficients may occur, potentially degrading system performance.

Computer wordlength selection is based upon design considerations that have their bases from fundamental engineering principles. This document has identified the following design considerations that are commonly addressed during computer wordlength selection.

DC12: Dynamic range and headroom are two computer wordlength considerations when A/D converters are specified.

DC13: Overflow, round-off/truncation, resolution, and type/size conversion of fixed- and floating-point numbers are potential sources of computer wordlength error.

DC14: Compatibility of analog output signals with downstream electrical/electronics systems are a consideration with D/A converter selection and installation. Areas of compatibility include signal shape, rate of change, range, and power level.

DC15: Finite wordlength effects on algorithm coefficients may affect the accuracy of computer calculations.

REFERENCES

ANSI/IEEE. Standard 279-1971, "Criteria for Protection Systems for Nuclear Power Generating Stations." New York: Institute of Electrical and Electronics Engineers, 1971.

ANSI/ISA. Standard S67.04-Part I-1994, "Setpoints for Nuclear Safety-Related Instrumentation." Raleigh, North Carolina: International Society of Measurement and Control, 1994.

Astrom, Karl J., and Bjorn Wittenmark. *Computer-Controlled Systems: Theory and Design*, 3rd ed. New York: Prentice Hall, 1997.

Clements, Alan. *Analog Interface and DSP Sourcebook*. New York: McGraw-Hill, 1993.

Daugherty, Kevin M. *Analog-to-Digital Conversion: A Practical Approach*. New York: McGraw-Hill, 1995.

EPRI, "Guidelines for Electromagnetic Interference Testing in Power Plants," EPRI TR-102323. Palo Alto, California: Electric Power Research Institute, 1994.

Franklin, G., J. Powell, and M. Workman. *Digital Control of Dynamic Systems*, 2nd ed. Reading, Massachusetts: Addison-Wesley, 1994.

GAO. "Patriot Missile Defense: Software Problem Led to System Failure at Dhahran, Saudi Arabia," GAO/IMTEC-92-26. Washington, D.C.: Government Accounting Office, February 1992.

Hoeschele, David F. *Analog-to-Digital and Digital-to-Analog Conversion Techniques*, 2nd ed. New York: John Wiley & Sons, 1994.

Houpis, C., and G. Lamont. *Digital Control Systems: Theory, Hardware, and Software*, 2nd ed. New York: McGraw-Hill, 1992.

IEEE. Standard 603-1991, "IEEE Standard Criteria for Safety Systems for Nuclear Power Generating Stations." New York: Institute of Electrical and Electronics Engineers, 1991.

IEEE. Standard 754-1985, "IEEE Standard for Binary Floating-Point Arithmetic." New York: Institute of Electrical and Electronics Engineers, 1985.

ISA. Standard S67.04-1982, "Setpoints for Nuclear Safety-Related Instrumentation Used in Nuclear Power Plants." Raleigh, North Carolina: International Society of Measurement and Control, 1982.

ISA. Standard RP67.04-Part II-1994, "Methodologies for the Determination of Setpoints for Nuclear Safety-Related Instrumentation." Raleigh, North Carolina: International Society of Measurement and Control, 1994.

ISA. ANSI/ISA-S67.06-1984, "Response-time Testing of Nuclear Safety-Related Instrument Channels in Nuclear Power Plants." Raleigh, North Carolina: International Society of Measurement and Control, 1984.

Lions, J. L. "Ariane 5: Flight 501 Failure." Paris: Inquiry Board, European Space Agency, July 1996.

Ludeman, Lonnie C. *Fundamentals of Digital Signal Processing*. New York: John Wiley & Sons, 1986.

National Semiconductor Corporation, "Specifying A/D and D/A Converters," Application Note 156. Arlington, Texas: National Semiconductor Corp., February 1976.

National Research Council. *Digital Instrumentation and Control Systems in Nuclear Power Plants: Safety and Reliability Issues*. Washington, D.C.: National Academy Press, 1997.

Nise, Norman S. *Control Systems Engineering*. Redwood City, California: The Benjamin/Cummings Publishing Co., 1992.

Nyquist, H. "Certain Topics in Telegraph Transmission Theory," *Trans. AIEE*, Vol. 47, April 1928.

REFERENCES

Pang, Chao-Sun. "Anti-Aliasing Filters and Data Validity: The Inside Story," *Sound and Vibration*, April 1998.

Phillips, Charles L., and H. Troy Nagle. *Digital Control Systems Analysis and Design*, 3rd ed. Englewood Cliffs, New Jersey: Prentice-Hall, 1995.

Razavi, Behzad. *Principles of Data Conversion System Design*. Piscataway, New Jersey: IEEE Press, 1995.

Shannon, C. E. "Communication in the Presence of Noise," *Proc. IRE*, Vol. 37, No. 1, January 1949.

Smith, Strether. *Digital Data Acquisition*. Santa Barbara, California: Tustin Technical Institute, 1998.

USNRC. "Instrument Setpoints for Safety-Related Systems," Regulatory Guide 1.105. Washington, D.C.: U.S. Nuclear Regulatory Commission, 1986.

USNRC. "Reviewing Real-Time Performance of Nuclear Reactor Safety Systems," NUREG/CR-6083. Washington, D.C.: U.S. Nuclear Regulatory Commission, 1993a.

USNRC. "Data Communications," NUREG/CR-6082. Washington, D.C.: U.S. Nuclear Regulatory Commission, 1993b.

USNRC. "Technical Basis for Evaluating Electromagnetic and Radio-frequency Interference in Safety-related I&C Systems," NUREG/CR-5941. Washington, D.C.: U.S. Nuclear Regulatory Commission, 1994.

USNRC. "Survey of Ambient Electromagnetic and Radio-frequency Interference Levels in Nuclear Power Plants," NUREG/CR-6436. Washington, D.C.: U.S. Nuclear Regulatory Commission, 1996b.

USNRC. "Chapter 7: Instrumentation and Control," *Standard Review Plan*, NUREG-0800. Washington, D.C.: U.S. Nuclear Regulatory Commission, 1997a.

USNRC. "Computer-based Digital System Failures: December 1996–March 1997," Memorandum from Jared Wermiel to Bruce Boger. Washington, D.C.: U.S. Nuclear Regulatory Commission, April 28, 1997b.

USNRC. "Recommended Electromagnetic Operating Envelopes for Safety-related I&C Systems in Nuclear Power Plants," NUREG/CR-6431. Washington, D.C.: U.S. Nuclear Regulatory Commission, 1997c.

USNRC. "Power/Flow Relationship Technical Specification Violation," Licensee Event Report, Docket No. 05000220. Washington, D.C.: U.S. Nuclear Regulatory Commission, 1998.

USNRC. "Recommendations for Reactor Oversight Process Improvements," SECY-99-007. Washington, D.C.: U.S. Nuclear Regulatory Commission, 1999.

Westphal, L.C. *Sourcebook of Control Systems Engineering*. New York: Chapman & Hall, 1995.

Williamson, Darrell. *Digital Control and Implementation: Finite Wordlength Considerations*. New York: Prentice-Hall, 1991.

GLOSSARY

Aliasing A phenomenon at analog-to-digital signal conversion, which results in some frequency components of the analog signal being misrepresented as components of lower frequency in the digital signal. Aliasing creates error between the analog signal and its digital representation.

Analog-to-Digital (A/D) Converter A device used in digital I&C systems to convert analog voltage signals to digital signals.

Analog-to-Digital (A/D) Transfer Function A graphical description of an A/D converter output value for a given input voltage level. It is often used to describe A/D converter errors.

Analog Multiplexer A device in digital I&C systems, which selects one analog signal from several input channels.

Anti-aliasing Filter A low-pass, analog filter that reduces the power of high frequency components in an analog signal, and thus, reduces the amount of aliasing in analog-to-digital conversion.

Band-limited Signal A signal in which all frequency components having non-zero magnitude are known to be below a particular frequency.

Bandwidth For signals, it is the span of frequencies that are of interest to a particular system. In signal filters, it is the span of frequencies in which the filter either allows these frequencies to pass through amplified or relatively unaltered.

Bit A place value in the binary numbering system. Wordlengths are typically denoted by the number of bits that compose them.

Closed-loop Bandwidth Method A sample rate selection method for closed-loop control systems that bases the sample rate on the closed-loop bandwidth of the analog control system.

Closed-loop I&C System Any I&C system that utilizes at least one feedback path within the system. The majority of systems within this category are closed-loop control systems.

Continuous I&C systems I&C systems whose input signals take on a range of values versus a discrete number of values.

Differential Nonlinearity (DNL) Error An A/D converter error that describes the amount of deviation from the expected transition in going from one binary state to another binary state.

Digital Signal A time-sequenced string of binary values representing a time-dependent quantity.

Digital-to-Analog (D/A) Converter A device used in digital I&C systems to convert digital signals into analog voltage signals.

Discrete I&C System I&C systems that receive discrete (on/off) input signals. These input signals typically come from devices such as relays, bistables, etc.

Dynamic Range (DR) The capability of an A/D converter to achieve both high resolution and a large input range.

Finite Wordlength Errors In digital systems, it is round-off/truncation errors, ignored overflow conditions, and inappropriate type/size conversions between/among numbering notations that add error to numerical computation of results. These errors originate from the computer's limited wordlength (see wordlength).

Frequency Spectrum Two graphs describing the sinusoidal components making up a signal. One graph plots sinusoidal magnitude versus frequency and the other plots phase shift versus frequency. Frequency spectrums are obtained from time-domain signals using the Fourier, Discrete Fourier, or Fast Fourier Transforms (see Appendix D).

Full-scale Error See gain error.

Gain Error When the voltage increment is greater or less than the ideal voltage increment between transition points for all binary codes. This causes the A/D transfer function slope to deviate from the ideal. Also called full-scale error.

Gain Margin The amount of control gain that can be added to a control system before instability occurs.

Headroom The ability of a digital I&C system to sample and acquire data points beyond the input signal's normal range.

Least-significant Bit (LSB) Error The resolution error present in all A/D converters due to the finite wordlengths of A/D converters.

Linearity Error The deviation from the ideal binary output transition points for increasing analog input in an A/D converter (see nonlinearity and differential nonlinearity error).

Low-pass Filter A signal filter allowing frequencies above a certain cutoff frequency to pass through relatively unaltered and attenuating the power of frequencies above the cutoff frequency.

Missing Code In A/D converters, it results in one binary output value skipped for an increasing input voltage.

Nonlinearity Error For A/D converters, it is the deviation between binary transitions in the actual and ideal A/D transfer functions.

Non-monotonicity A decrease in the binary output for an increase in the input voltage.

Non-safety System Systems that are not safety systems (see safety-related system).

Nyquist Frequency The frequency equal to half of the sample rate. In digital sampling systems, signal frequency components above the Nyquist frequency "fold" on top of those frequencies below the Nyquist frequency.

Offset Error In A/D converters, a right or left shift in the A/D transfer function due to amplifier offsets, ground problems, or internal malfunctions. Also called zero error.

Open-loop I&C System Systems that do not utilize a feedback signal as part of its operation. These systems accept input signals, process the signals, and deliver an output. Typical open-loop I&C systems include monitoring, protection, alarm, and some control systems.

Overflow In computers, it is the case in which the addition of two numbers produces a result whose size exceeds that of the computer's wordlength by 1 bit (see bit and wordlength).

Overflow Noise Discontinuous jumps in the output of a digital I&C system as a result of ignoring overflow conditions.

Oversampling Method A sample rate selection method that relies upon very fast sample rates to keep aliasing to a minimum.

Phase Margin The amount of phase shift that needs to be added to a control system to make it unstable.

Phase/Gain Margin Method A sample rate selection method for closed-loop control systems, which bases the sample rate on meeting stated phase and gain margin goals for the digital control system.

Rise-time Method A sample rate selection method for both open- and closed-loop I&C systems, which bases the sample rate on the rise time of the analog I&C system output. The rise-time method is not preferred in safety systems that require signal accuracy.

Safety-related System Those systems that are relied upon to remain functional during and following design basis events to assure: (1) the integrity of the reactor coolant pressure boundary; (2) the capability to shut down the reactor and maintain it in a safe shutdown condition; or (3) the capability to prevent or mitigate the consequences of accidents which could result in potential offsite exposures (adapted from 10 CFR 50.2 definition for safety-related systems, components, and structures).

Sample Rate The frequency at which an analog signal is sampled and converted to a binary number.

Sampling Ratio (SR) The ratio of the sample rate over the maximum frequency in the bandwidth of an input signal. In the sampling ratio method, various

anti-aliasing filters have their own sampling ratio to limit aliasing to a maximum level in the digital signal. That sampling ratio is multiplied by the maximum bandwidth frequency to obtain the sample rate.

Sampling Ratio Method A sample rate selection method for open-loop I&C systems that relies on the high frequency attenuation capabilities of an anti-aliasing filter to maintain aliasing below a required limit.

Shannon's Sampling Theorem A theorem stating that, in order to avoid aliasing, the sample rate must be two times faster than the highest frequency in the analog signal.

Signal Bandwidth See Bandwidth.

Spectrum Analyzer A device measuring the magnitude of the frequency components in a signal.

Wordlength A finite number of bits used to represent a single numerical value in a computer. Typical wordlengths are 8, 16, and 32 bits for computers and 8, 10, 12, 14, 16, 20, 22, and 24 bits in A/D converters.

Zero Error See offset error.

APPENDIX A: A/D CONVERTERS

Analog-to-digital (A/D) converters sample input voltage signals and represent the samples using binary numbers. The binary numbers are then used by digital I&C systems to perform monitoring, protection, alarm, and control functions. This appendix describes the operation and features of six common types of A/D converters:

- successive-approximation A/D converter
- tracking A/D converter
- integrating (dual ramp) A/D converter
- parallel (flash) A/D converter
- voltage-to-frequency converter
- sigma-delta A/D converter

This appendix gives precautions and limitations for each converter; general error specifications covering all A/D converters are given in Chapter 3.

Successive-approximation A/D Converters

Successive-approximation A/D converters use a binary search scheme to determine the input voltage signal (Philips and Nagle, 1995). Key components are a digital-to-analog (D/A) converter, comparator, clock, and control unit. Figure A.1 is a block diagram of the successive-approximation A/D converter. The D/A converter produces a reference voltage proportional in magnitude to the binary output value of the A/D. This provides feedback, which allows the A/D converter to compare its binary search guess to the input voltage. Using the clock and the comparator output, the control unit guides the binary search. Operation of the successive-approximation A/D converter is seen through the following example.

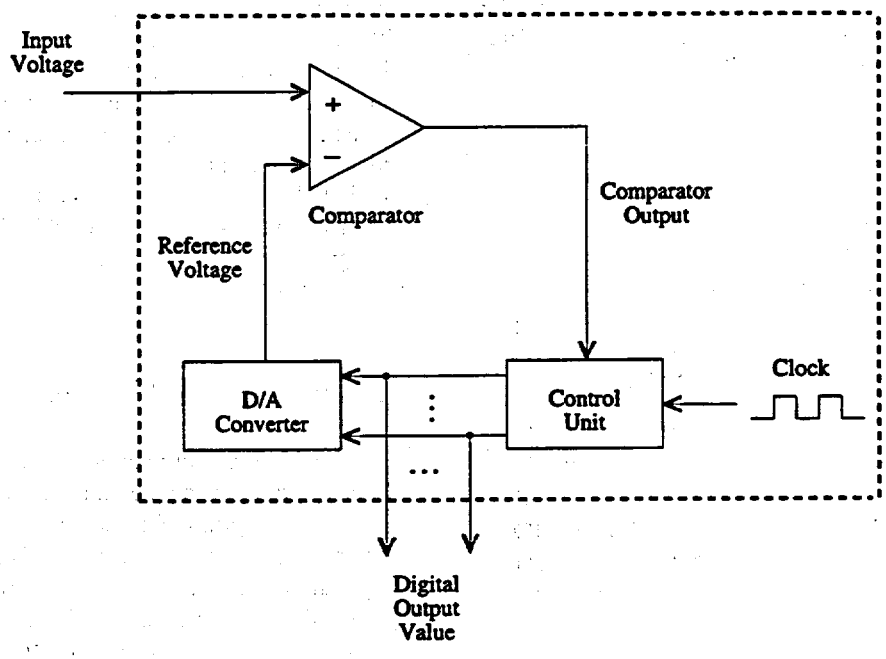


Figure A.1 Successive-approximation A/D converter

An example illustrating the operation of a successive-approximation A/D converter is given in Figure A.2 (Clements, 1993; Hoeschele, 1994; Philips and Nagle, 1995). In the example, a 3-bit successive-approximation A/D converter, with an input range of 0 to 10V, samples a 6.5V input value. The binary search scheme starts with the most significant bit and proceeds to the least significant bit. Transition from one bit to another is controlled by a clock. When a sample is initiated, the control unit sets all digital output bits to 0 except for the most significant bit, which is set to 1. This binary value, "100," is sent to the D/A converter, which generates a reference voltage of 5V. Since 5V is less than 6.5V, the comparator output is 1. The comparator output value signals the control unit to keep the most significant bit set. The next significant bit is determined by setting that bit to 1, and sending the binary result, "110," to the D/A converter. The D/A converter generates 7.5V, which is larger than 6.5V. The comparator output signals the control unit to clear that bit. To determine the final bit, the control unit sets the least significant bit, combines it with the previous results, and sends the binary result to the D/A converter. The value sent to the D/A converter is "101," which generates 6.25V. Since 6.25V is lower than 6.5V, the comparator signals the control unit to keep the least significant bit set. The final binary output value is "101."

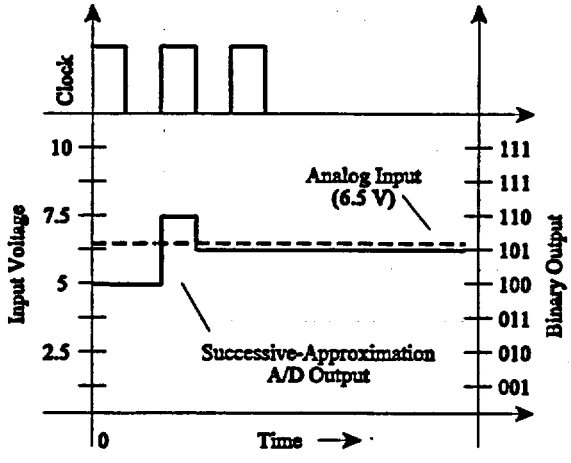


Figure A.2 Successive-approximation A/D converter example

In successive-approximation A/D converters, each bit is determined using previously identified bit values and testing the current bit in question. The order of determining bit values is from the most significant bit to the least significant bit. If the reference voltage is greater than the input voltage, the bit in question is set to 0. If the reference voltage is less than the input voltage, the bit in question remains at binary 1. Notice in the example that it takes three steps to determine the binary result. For successive-approximation A/D converters, it takes N steps to complete the conversion, where N is the number of bits in the binary result.

The binary search scheme used by the successive-approximation A/D converter requires the input voltage to remain constant during the conversion process. In practice, it takes a small amount of time to perform the A/D conversion, and during this time, the input voltage changes. A sample-and-hold circuit clamps the analog input value to its instantaneous value when the conversion process begins.

Sample-and-hold circuits use a switch and capacitor combination to hold the input voltage. Figure A.3 illustrates a sample-and-hold circuit and its operation (Hoeschele, 1994). When the switch is closed, the output voltage follows the input voltage. During this time, the capacitor has the same value as the input. When a sample is initiated at time T_1, the switch opens and the capacitor retains the value of the input signal right before the switch was opened. Although the sample-and-hold circuit can be located external to the A/D converter chip, it is commonly integrated into successive-approximation A/D converter chips.

Tracking A/D Converters

Tracking A/D converters continuously update their binary output, even when there is not a sample request. The block diagram of a tracking A/D converter is given in Figure A.4 (Phillips and Nagle, 1995). Operation of a tracking A/D converter is similar to a successive-approximation A/D converter except that it uses a counter to command the D/A converter reference voltage. For example, if the unknown input voltage is greater than the voltage provided by the D/A

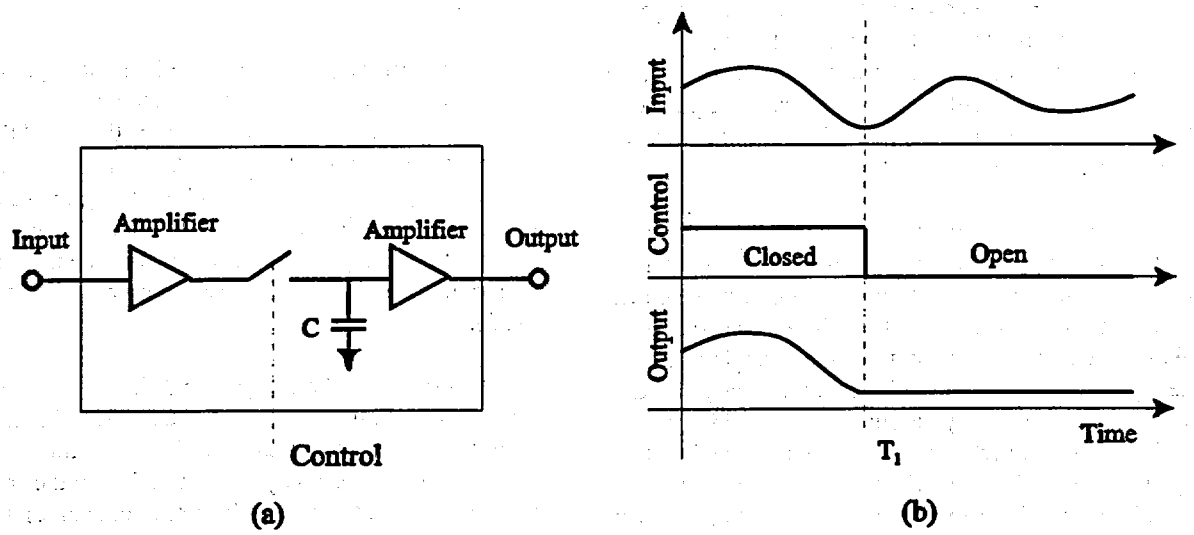


Figure A.3 Sample-and-hold: (a) simplified circuit and (b) timing diagram

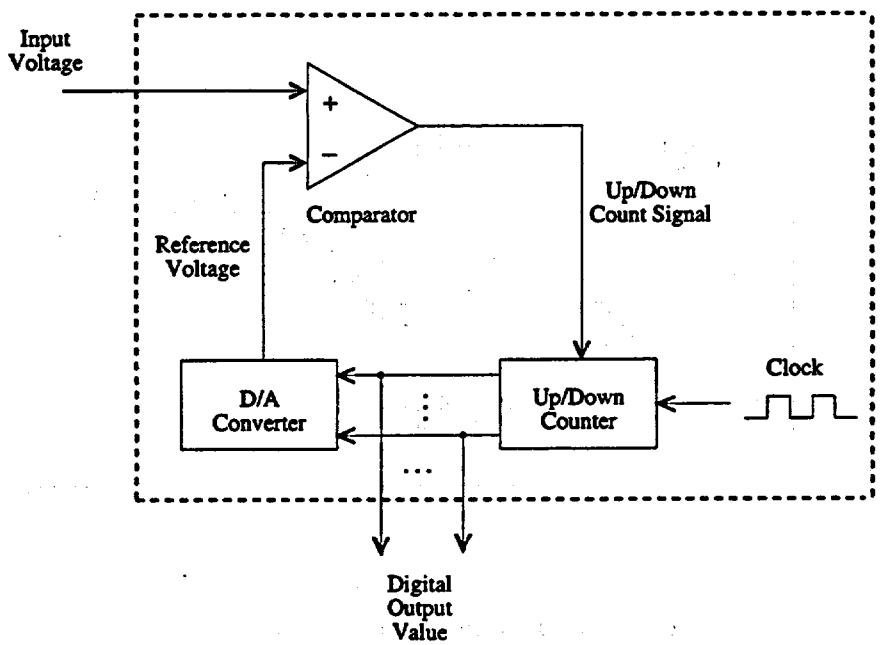


Figure A.4 The tracking A/D converter

converter, the comparator commands the up/down counter to increment. Since the input to the D/A converter is the counter value, the reference voltage increases to track the input voltage. If the input voltage is lower than the reference voltage, the counter decrements. The count value is the binary output of the tracking A/D converter, and it is accessible at any time after the converter is initialized.

There are two precautions when using tracking A/D converters. One precaution involves converter initialization, and the other relates to input voltage rate of change. When the converter is first initialized, it takes some unknown amount of time to begin tracking the input voltage. During this time, the binary output is incorrect. The binary output is also invalid if the tracking A/D converter is not able to track the input signal due to rapid signal changes. In general, if the rate of change of the analog signal is less than ±1 least significant bit times the clock frequency, the tracking A/D converter may be used (Clements, 1993). Both initialization and rate-of-change problems are illustrated in Figure A.5.

Integrating (Dual-Ramp) A/D Converters

The working principle of the integrating, or dual ramp, A/D converter is to integrate the unknown voltage signal for a known amount of time, and then reverse the integral value with a known reference voltage. Figure A.6 provides a block diagram of an integrating A/D converter, which consists of an analog integrator, a comparator, a counter for time tracking, and logic to control the conversion process (Clements, 1993).

Operation of the integrating A/D converter is illustrated in Figure A.7 (Clements, 1993). First, the input voltage is integrated for a fixed amount of time, T_1, which is measured by a counter. When the counter overflows (counts one past its maximum value), the counter resets and continues counting. At the same time, the input to the integrator is switched from the input voltage to a reference voltage, V_{REF}. The magnitude of V_{REF} is equal to the maximum possible

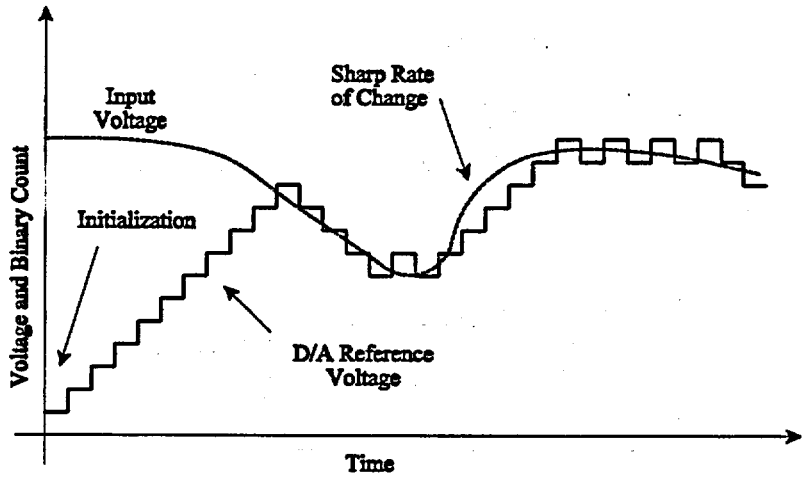


Figure A.5 Tracking A/D converter operation

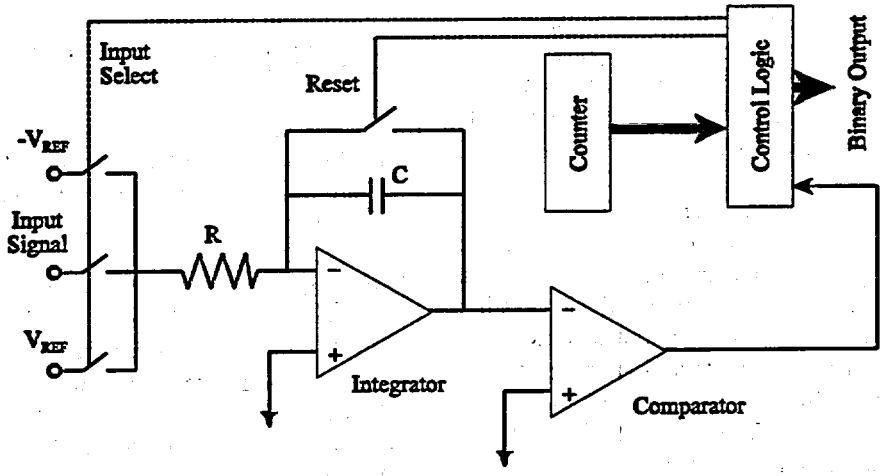


Figure A.6 Integrating (dual ramp) A/D converter

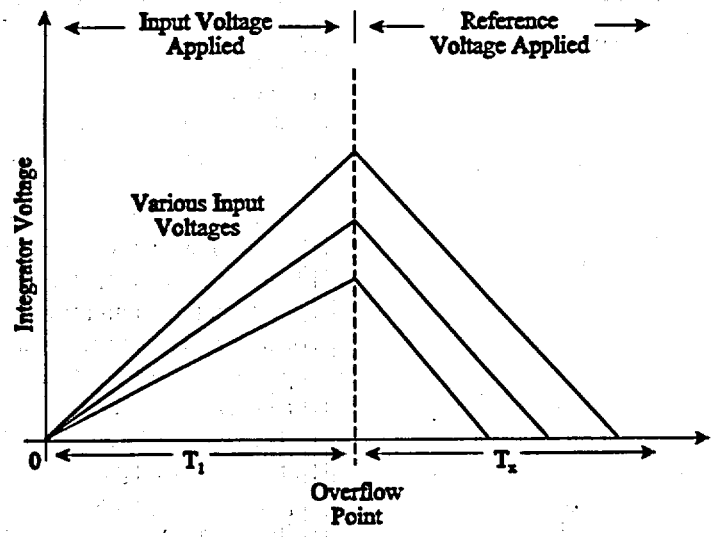


Figure A.7 Integrating (dual ramp) A/D converter operation

value of the input voltage, and its polarity is opposite of the input voltage's polarity. The object is to drive the integral value back to zero. Since V_{REF} is equal to the maximum expected voltage, the time, T_x, it takes to drive the integral value back to zero is less than or equal to the amount of time it took to integrate the input voltage. Therefore, the counter value when the integral becomes zero is the average value of the input voltage over the sample period.

The integrating A/D converter has several advantages over other A/D converters. First, it does not require a sample-and-hold circuit since it integrates the input over a period of time. Second, the integrating A/D converter is capable of notching out specific frequencies depending on the integration time period, T_1. Figure A.8 is the frequency response of an integrating A/D converter (Daugherty, 1995). The frequency response has a -20dB/decade roll-off to help with aliasing concerns, in addition to notching out frequencies at multiples of $1/T_1$. In many applications, $T_1 = 1/60$ to attenuate 60 Hz noise and its harmonics.

Normally, the integrating A/D converter requires more time to perform the A/D conversion compared to other converters. Therefore, it may not be suitable for applications requiring fast sample rates. Also, voltage offsets between the input and reference voltage cause errors in these converters. These offsets come from improper grounding or electrical noise (Clements, 1993).

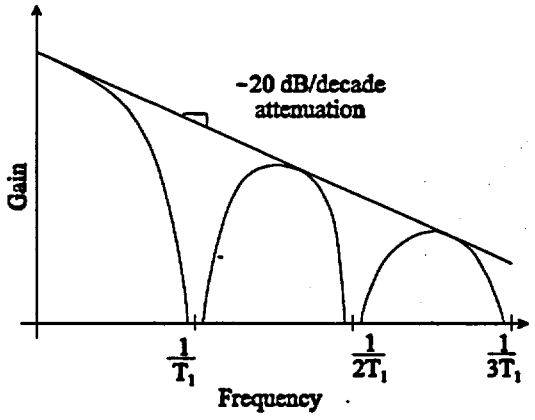


Figure A.8 Frequency response of the integrating A/D converter

Parallel (Flash) A/D Converters

When very fast conversion rates are needed, a parallel A/D converter is often used. Instead of determining each bit value one at a time, as in the successive-approximation A/D converter, all bit values are found simultaneously. Figure A.9 illustrates a 3-bit parallel converter using seven comparators (Phillips and Nagle, 1995). An *n*-bit parallel converter requires $2^n - 1$ comparators to operate. The reference voltage for each comparator is controlled by a resistor network. The comparative results are processed by combination logic to arrive at the binary output value. Although it is fast, it is often used with sample-and-hold circuits to achieve accurate results.

Voltage-to-Frequency Converters

Voltage-to-frequency (V/F) converters are integrating types of A/D converters commonly used for slow-changing signals. Instead of binary values, these converters send a train of pulses to the processing unit. The processing unit counts the number of pulses over a time period and uses the count value to represent the analog input. The count value is proportional to the average input voltage for the given time period.

The most common type of V/F converter is the charge-balancing V/F converter (Hoeschele, 1994). Figure A.10 provides the circuit block diagram and operational diagram for the charge-balancing V/F converter. The converter operates by charging the capacitor, C, to a positive voltage using the reference current I_R. The charging occurs for a fixed amount of time called the "reset" period. After the reset period, t_R, the input voltage, V_I, is integrated until the capacitor voltage becomes zero. When the capacitor voltage reaches zero, one pulse is sent out, and the V/F converter begins another reset period. The smaller the input voltage, the more time between output pulses.

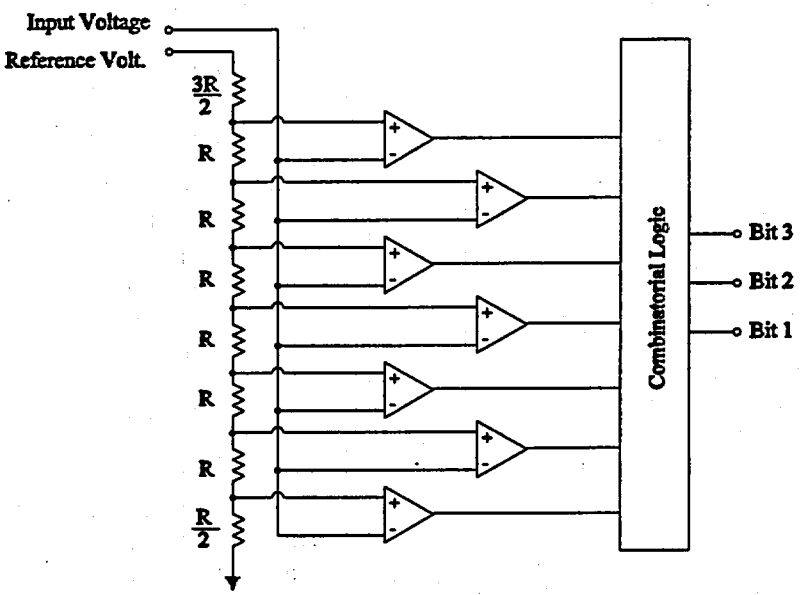


Figure A.9 Parallel (flash) A/D converter

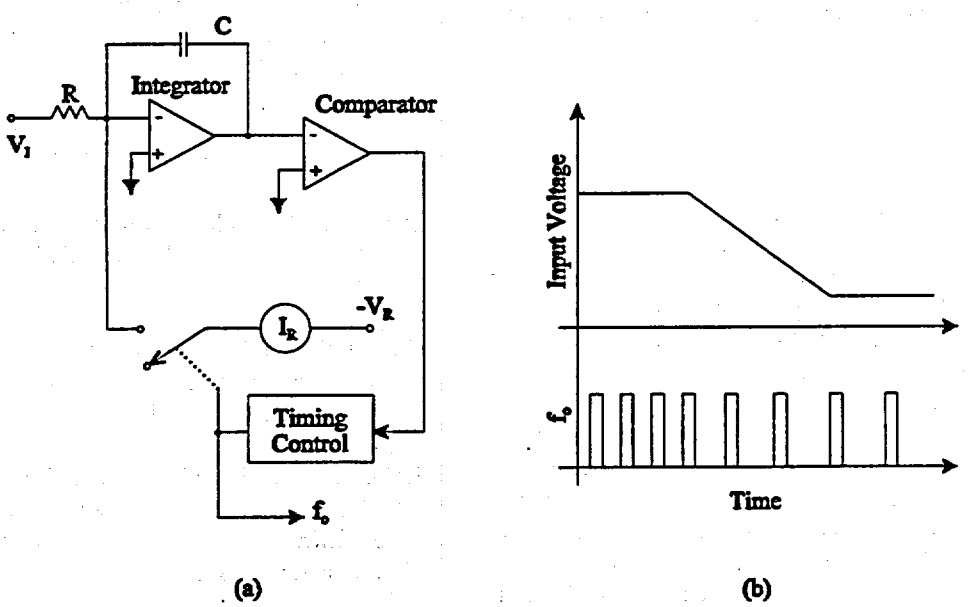


Figure A.10 Voltage-to-frequency converter: (a) diagram and (b) operation

The pulse frequency, f_o, for a charge-balancing V/F converter is determined through the following equation

$$f_o = \frac{V_I}{R \cdot t_R \cdot I_R}$$

where R is the integrator resistance, t_R is the reset time period, and I_R is the reference current. Errors in the output frequency are affected by the three terms in the denominator. The reset time period is normally controlled by an analog ramp circuit, which provides good timing resolution for each reset period. Resistance is mainly affected by tolerances and temperature drift. The reference current has the largest effect on frequency error, and it is specified in V/F converter data sheets.

V/F converters possess good noise rejection capabilities due to the integration process. Because of this capability, they are often used in industrial applications. The V/F converter frequency response has a -20dB/decade attenuation slope, and it is capable of notching out frequencies at integer multiples of the sampling frequency. It is similar to the frequency response of the integrating A/D converter, as shown in Figure A.8 (Garrett, 1981).

Sigma-Delta A/D Converters

Sigma-delta A/D converters contain low resolution A/D converters (typically 1bit), but achieve high resolution through a combination of fast sampling and digital filtering (Candy, 1992; Hein, 1993; Norsworthy et al., 1997). In Figure A.11(a), the sigma-delta A/D converter creates a pulse train representing the analog input (Daugherty, 1995). The pulse train, C_{OUT}, feeds a 1-bit D/A converter and a digital filter. The purpose of the D/A converter is to provide feedback, which enables tracking of the input signal. The integrator/comparator combination drives the difference between the input and pulse-train estimate to zero. Figure A.11(b) illustrates tracking of the input and the resulting pulse train output (Norsworthy et al., 1997).

The digital filter creates longer data wordlengths and reduces the amount of data. Figure A.12 illustrates one type of digital filter used in sigma-delta A/D converters. The finite-impulse response (FIR) filter performs a moving average on a finite number of data points. The FIR filter creates an 8 bit wordlength, while at the same time attenuating high frequencies. Data reduction is accomplished by keeping every n^{th} data point from the FIR filter output, and throwing away the rest. This type of data reduction is called decimation. Since the FIR filter attenuates higher frequencies, aliasing does not add significant errors to the signal. If further data reduction is needed, additional filter and sampling stages are added.

Sigma-delta A/D converters are gaining popularity because they provide high resolution and larger data throughput. Because sigma-delta A/D converters sample very fast, aliasing is less of a problem. However, it is still good practice to use an RC filter to prevent the possibility of aliasing errors (Pang, 1998).

References

Candy, James, and Gabor Temes, eds. *Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation*. Piscataway, New Jersey: IEEE Press, 1992.

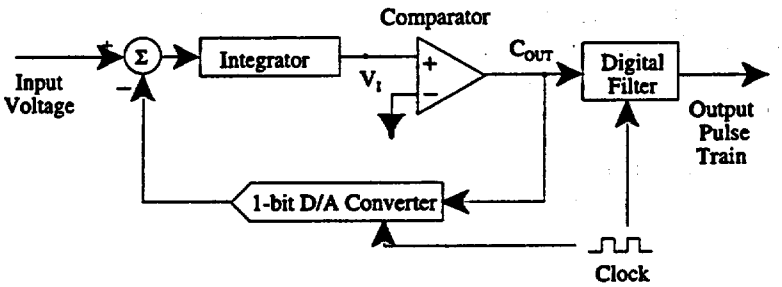
Clements, Alan. *Analog Interface and DSP Sourcebook*. New York: McGraw-Hill, 1993.

Daugherty, Kevin M. *Analog-to-Digital Conversion: A Practical Approach*. New York: McGraw-Hill, 1995.

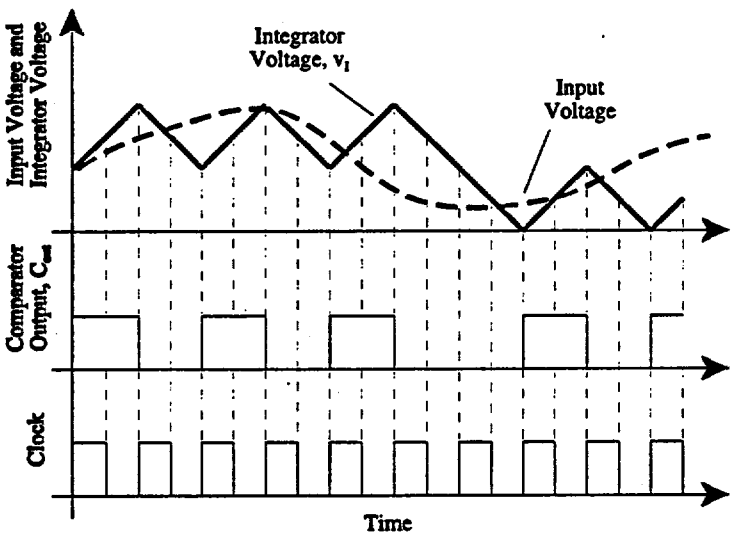
Garrett, Patrick H. *Analog I/O design : Acquisition, Conversion, Recovery*. Reston, Virginia: Reston Publishing Co., 1981.

Hein, Soren, and Avideh Zakhor. *Sigma-delta Modulators: Nonlinear Decoding Algorithms and Stability Analysis*. Boston: Kluwer Academic Publishers, 1993.

Hoeschele, David F., Jr. *Analog-to-Digital and Digital-to-Analog Conversion Techniques*, 2nd ed. New York: John Wiley & Sons, 1994.



(a)



(b)

Figure A.11 Sigma-delta A/D converter: (a) diagram and (b) operation

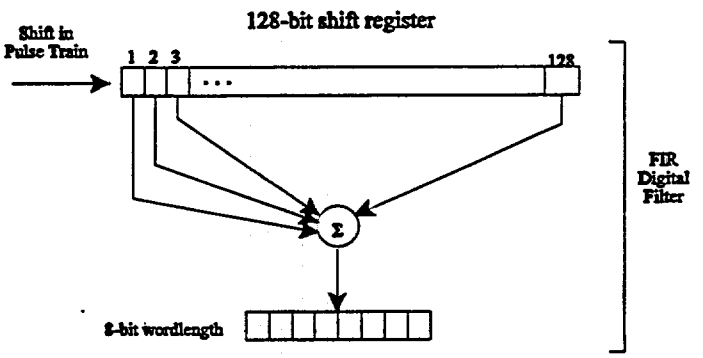


Figure A.12 Illustration of the digital filter found in a sigma-delta A/D converter

Norsworthy, Steven, Richard Schreier, and Gabor Temes, eds. *Delta-Sigma Data Converters: Theory, Design, and Simulation.* Piscataway, New Jersey: IEEE Press, 1997.

Pang, Chao-Sun. "Anti-aliasing Filters and Data Validity: The Inside Story," *Sound and Vibration,* April 1998.

Phillips, Charles L., and H. Troy Nagle. *Digital Control System Analysis and Design,* 3rd ed. Englewood Cliffs, New Jersey: Prentice-Hall, 1995.

APPENDIX B: SHANNON'S SAMPLING THEOREM

Shannon's Sampling Theorem is key to avoiding digital instrumentation and control (I&C) system failure caused by aliasing. Appendix B presents the theoretical background leading to Shannon's Sampling Theorem. The technical basis found in this appendix supports regulatory decisions regarding sample rate selection in nuclear I&C systems.

Digital Signal Representation

Developing a mathematical basis for the sampling theorem requires an A/D converter model. The entity modeling the A/D converter is the ideal sampler. An ideal sampler is simply a switch, taking instantaneous values of analog signals. The ideal sampler provides a simple mathematical model allowing straightforward derivation of Shannon's Sampling Theorem (Phillips and Nagle, 1995).

There are two differences between the ideal sampler and A/D converter. First, the ideal sampler assumes the sample is taken instantaneously; however, the A/D converter takes a small amount of time (on the order of nanoseconds) to obtain a sample. Second, the ideal sampler provides the actual value of the analog signal, while the A/D converter provides a rounded value due to the converter's finite wordlength. However, neither difference prohibits the ideal sampler from modeling A/D converters.

Figure B.1 illustrates the function of an ideal sampler. In the figure, an analog signal, p(t), is sampled at a constant time interval using the ideal sampler. The resulting digitized signal is p*(t).

The ideal sampler is mathematically represented with the *unit impulse function*, $\delta(t)$. The unit impulse function, also known as the Dirac delta function, has three properties (Jackson, 1991):

- an amplitude, A, approaching infinity
- a pulse width, W, approaching zero
- the area equal to one under the function

The unit impulse function has value only at time equal to zero. The definition of the unit impulse function is graphically illustrated in Figure B.2(a). The mathematical symbol for the unit impulse function is shown in Figure B.2(b). And, the unit impulse function can be time-shifted by an amount, τ, as shown in Figure B.2(c).

The ideal sampler is modeled by a sum of unit impulse functions time-shifted by the sample period, T (Phillips and Nagle, 1995):

$$\delta_T(t) = \delta(t) + \delta(t-T) + \delta(t-2T)... \qquad \text{(B-1)}$$

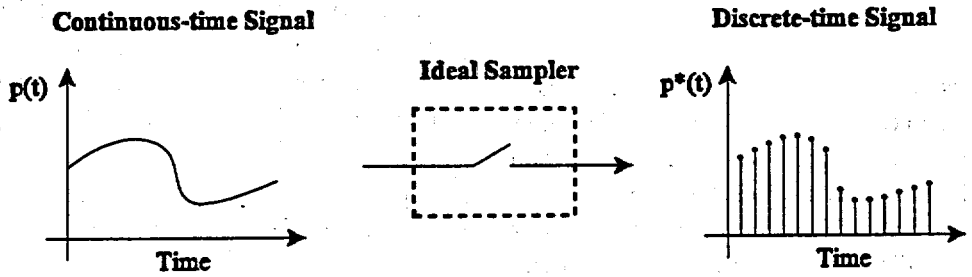


Figure B.1 The ideal sampler

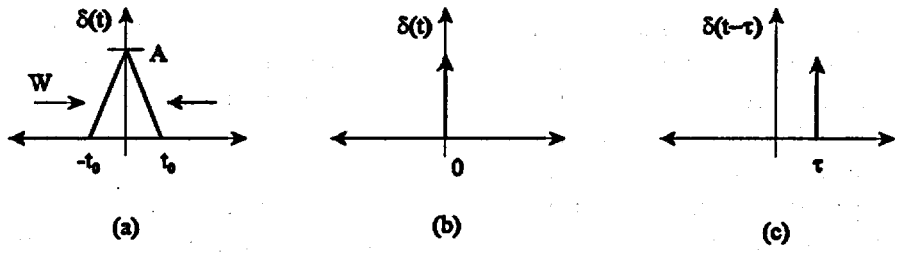


Figure B.2 The unit-impulse function: (a) definition of the unit impulse function; (b) unit impulse function symbol; (c) time-shifting of the unit impulse function

Consider a continuous-time signal, p(t). If p(t) is sampled, only the values of p(t) at the sample instances are known. The sampled version of p(t) is represented by $p^*(t)$. Mathematically, $p^*(t)$ is represented by a series of time-shifted, unit impulse functions (Eq. B-1) all weighted by the instantaneous value of p(t):

$$\begin{aligned} p^*(t) &= p(t)\cdot\left[\delta(t)+\delta(t-T)+\delta(t-2T)+\ldots\right] \\ &= p(0)\delta(t)+p(T)\delta(t-T)+p(2T)\delta(t-2T)+\ldots \\ &= p(t)\sum_{k=-\infty}^{\infty}\delta(t-kT) \end{aligned} \qquad \text{(B-2)}$$

Equation B-2 represents the output of the ideal sampler. The unit-impulse functions appearing at the output of the sampler are "ideal," hence the name "ideal sampler."

Sampling Viewed in the Frequency Domain

The effects of sampling are best illustrated in the frequency domain (Franklin et al., 1994). In Equation B-2, the output of the sampler is represented by a train of unit impulse functions multiplied by the continuous-time signal. Since the train of unit impulse functions is periodic, it can be represented by a Fourier series

$$\sum_{k=-\infty}^{\infty}\delta(t-kT)=\sum_{n=-\infty}^{\infty}C_n e^{j\left(\frac{2\pi n}{T}\right)t} \qquad \text{(B-3)}$$

with the Fourier coefficients, C_n, calculated by

$$C_n=\frac{1}{T}\int_{-T/2}^{T/2}\left(\sum_{k=-\infty}^{\infty}\delta(t-kT)\cdot e^{-jn\left(\frac{2\pi t}{T}\right)}\right)dt \qquad \text{(B-4)}$$

In Equation B-4, the integral for the Fourier coefficients is over one period, so the only unit impulse function of interest is the one at the origin, δ(t).

$$C_n=\frac{1}{T}\int_{-T/2}^{T/2}\left(\delta(t)\cdot e^{-jn\left(\frac{2\pi t}{T}\right)}\right)dt=\frac{1}{T} \qquad \text{(B-5)}$$

Since δ(t) only has value at zero, and the area under δ(t) is one, the integral reduces to unity, and $C_n = 1/T$. Using the result of Equation B-5, and substituting it into Equation B-3 results in the following:

$$\sum_{k=-\infty}^{\infty}\delta(t-kT)=\frac{1}{T}\sum_{n=-\infty}^{\infty}e^{j\left(\frac{2\pi n}{T}\right)t} \qquad \text{(B-6)}$$

The sampling rate, $\omega_s = 2\pi/T$, is substituted into Equation B-6. The Fourier series representation of the train of unit impulse functions (Eq. B-6) is then substituted into Equation B-2:

$$p^*(t) = p(t) \cdot \left[\frac{1}{T} \sum_{n=-\infty}^{\infty} e^{jn\omega_s t} \right] \qquad \text{(B-7)}$$

The Laplace transform is taken of Equation B-7:

$$L\left[p^*(t)\right] = \int_{-\infty}^{\infty} p(t) \cdot \left[\frac{1}{T} \sum_{n=-\infty}^{\infty} e^{jn\omega_s t} \right] \cdot e^{-st} dt \qquad \text{(B-8)}$$

Moving the summation outside the integral and combining exponentals, Equation B-8 becomes:

$$P^*(s) = \frac{1}{T} \sum_{n=-\infty}^{\infty} \int_{-\infty}^{\infty} p(t) \cdot e^{-(s - jn\omega_s)t} dt \qquad \text{(B-9)}$$

The integral term in Equation B-9 is the Laplace transform of p(t) with a shift in frequency. This equation could also be written as:

$$P^*(s) = \frac{1}{T} \sum_{n=-\infty}^{\infty} P(s - jn\omega_s) \qquad \text{(B-10)}$$

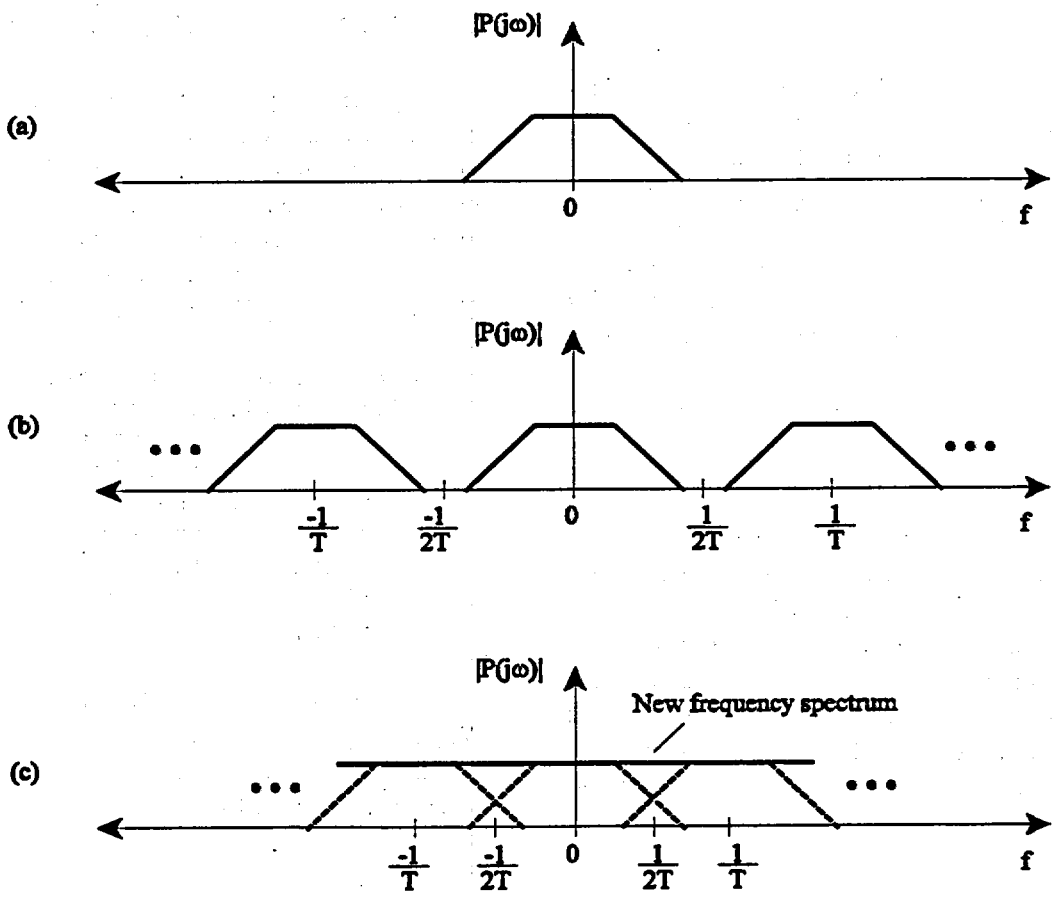


Figure B.3 Frequency spectrum view of: (a) an analog signal, (b) the sampled version of the analog signal, and (c) an aliased version of the sampled signal

The result in Equation B-10 provides great insight into sampling. A sampled version of p(t) contains the original frequency spectrum of the continuous-time signal, plus infinite copies of the frequency spectrum centered at multiples of the sampling rate, ω_s. Figure B.3(a) illustrates the frequency spectrum for a continuous-time signal, p(t). In Figure B.3(b), multiple copies of the frequency spectrum appear in the sampled signal. If an ideal low-pass filter existed, the original frequency spectrum of p(t) could be recovered from the sampled signal. In practice, D/A converters act as low- pass filters by reconstructing the analog signal. While there is some corruption/loss of data due to non-ideal properties of the D/A converter, most data from the continuous-time signal is recovered successfully.

In Figure B.3(b), copies of the frequency spectrum are distinguishable one from another. In Figure B.3(c), the copies overlap, forming a new frequency spectrum. Even with an ideal low-pass filter, the original frequency spectrum cannot be recovered. In this case, data from the continuous-time signal is corrupted. The overlap is caused by a sampling frequency, ω_s, too low for the given analog signal. This type of signal error is known as *aliasing*.

Sampling Viewed in the Time Domain

In the time domain, aliased signals have high frequency data masked as low frequency data. Figure B.4 illustrates of the effects of aliasing in the time domain. In the figure, the solid-line sine wave is sampled once per period. The dotted-line sine wave has a lower frequency, but with the given samples, it can also fit the samples. In this case, the digital I&C system views the sampled sine wave as having a lower frequency instead of its correct frequency.

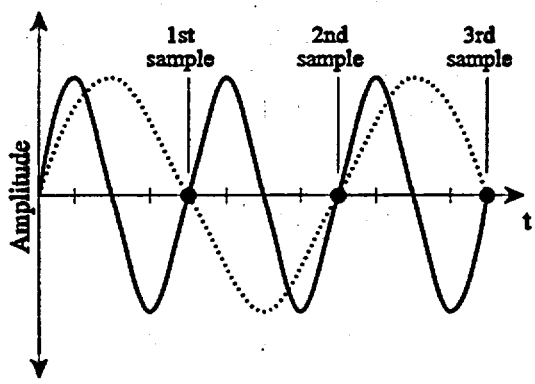


Figure B.4 Aliasing in the time domain

Shannon's Sampling Theorem

By increasing the sample frequency, copies of the original frequency spectrum increase in distance from one another until there is no overlap. To prevent overlap in the frequency spectrum, the sample rate is required to be greater than two times the maximum frequency in the continuous-time signal. This leads to Shannon's Sampling Theorem (Shannon, 1949):

> Consider a continuous-time signal p(t) with the highest frequency component f_o Hertz, and assume that this is sampled at a frequency f_s Hertz. Then it is possible to reconstruct p(t) from its sampled version $p^*(t)$ if, and only if, $f_s > 2f_o$.

The frequency, f_o, is the Nyquist rate, or the *Nyquist frequency*. Any frequencies in the analog signal above the Nyquist frequency are aliased during sampling (Ludeman, 1986).

Theory vs. Practice in Digital Sampling

Shannon's Sampling Theorem considers ideal conditions. First, it assumes the analog signal is band-limited (Ludeman, 1986). In band-limited signals, all frequency components with non-zero magnitude are below a certain frequency. In practical applications, high frequencies exist in analog signals due to electrical noise or process/component dynamics. Although these high frequencies can be reduced by anti-aliasing filters, they cannot be eliminated. Since high frequencies cannot be eliminated, some amount of aliasing occurs.

References

Franklin, G., J. Powell, and M. Workman. *Digital Control of Dynamic Systems*, 2nd ed. Reading, Massachusetts: Addison-Wesley, 1994.

Jackson, Leland B. *Signals, Systems, and Transforms*. Reading, Massachusetts: Addison-Wesley, 1991.

Phillips, Charles L., and H. Troy Nagle. *Digital Control System Analysis and Design*, 3rd ed. Englewood Cliff, New Jersey: Prentice-Hall, 1995.

Ludeman, Lonnie C. *Fundamentals of Digital Signal Processing*. New York: John Wiley & Sons, 1986.

Shannon, C.E., "Communication in the Presence of Noise," *Proc. IRE*, Vol. 37, No. 1, January 1949.

APPENDIX C: ANTI-ALIASING FILTERS

Anti-aliasing filters attenuate or reduce the power of unwanted high frequencies to minimize aliasing error. Anti-aliasing filters are analog low-pass filters placed directly in front of A/D converters (Smith, 1998). Since the frequency response of a low-pass filter is approximately one at low frequencies, the anti-aliasing filter allows low frequencies to pass through with minimal changes. At high frequencies, the gain of the low-pass filter decreases, and high frequency components are reduced in power. When attenuated high frequencies are aliased, they do not add as much error to the sampled signal as they would have otherwise.

Figure C.1 illustrates the frequency response of an anti-aliasing filter. The horizontal axis denotes frequency and the vertical axis denotes filter gain. The passband (or bandwidth) is the portion of the anti-aliasing filter allowing low frequencies to pass through the filter. To keep the magnitude of "passed" frequencies the same, the passband gain is unity. The cutoff frequency, f_c, is the point at which the passband ends and the attenuation slope begins. At the cutoff frequency, the gain of the filter drops to -3dB (1/2 power, 0.707 original magnitude). The attenuation slope shows how fast the gain of the filter decreases as the frequency increases. The ideal attenuation slope is negative infinity, but it is not possible in practice. The stopband characterizes the gain of the filter for frequencies past the attenuation slope. For anti-aliasing filters, the stopband gain should be as low as possible.

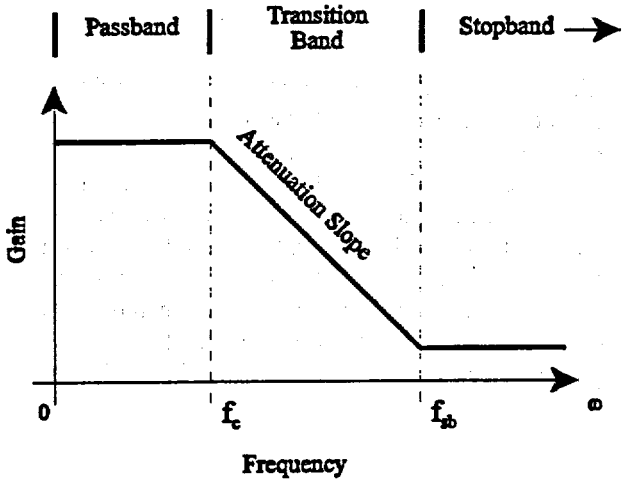


Figure C.1 Anti-aliasing filter definitions

Types of Anti-aliasing Filters

There are several types of anti-aliasing filters, each with its own benefits. Anti-aliasing filters are described by their type and the number of poles they contain in their transfer function. Common types of anti-aliasing filters are the RC filter, Bessel, Butterworth, and Elliptical (Cauer) filters (Smith, 1998). The following is a description of each type of filter.

RC Filter: The RC filter, or single-pole filter, is the simplest anti-aliasing filter. The top plot in Figure C.2 illustrates the frequency response of the RC filter. RC filters provide a -20dB per decade attenuation slope, requiring the cutoff frequency to be set below 1 Hz for most applications. This ensures 60 Hz noise and its associated harmonics are adequately suppressed (Smith, 1998). The benefit of an RC filter is its simple construction, but it has the worst attenuation slope of all filters.

Bessel Filter: Bessel filters are a type of complex filter. Complex filters contain multiple poles and may contain zeros in their transfer function. The Bessel filter offers uniform delay to all frequencies, meaning there is little overshoot in the time domain. However, this filter has the poorest passband uniformity and the slowest attenuation slope of all complex filters. The middle plot of Figure C.2 illustrates the frequency response of a 2-, 4-, and 6-pole Bessel filter. Increasing the number of poles increases the attenuation slope of the filter.

Butterworth Filter: Butterworth filters provide an improvement over the Bessel filter, and they are commonly used as anti-aliasing filters. The Butterworth filter provides excellent passband uniformity and a sharper attenuation slope. However, the Butterworth filter provides these improvements at the cost of introducing more overshoot in the time domain. The bottom plot of Figure C.2 illustrates the frequency

response of 2-, 4-, and 6-pole Butterworth filters. Again, increasing the number of poles for the Butterworth filter increases the attenuation slope.

Elliptical/Cauer Filter: Elliptical filters provide the best attenuation slope of all the complex filters. However, the elliptical filter has different characteristics compared to the other complex filters. For example, the elliptical filter has good passband uniformity across the bandwidth, but it does contain small ripples. In addition to the passband ripple effect, the gain bounces in the stopband. Fortunately, these characteristics do not significantly affect its performance as an anti-aliasing filter. The elliptical filter is able to provide a very steep attenuation slope at the expense of large oscillations in the time domain. The elliptical filter is often used in high-performance data acquisition systems. Figure C.3 illustrates the frequency response of a 6-pole/6-zero elliptical filter.

Reference

Smith, Strether. *Digital Data Acquisition.* Santa Barbara, California: Tustin Technical Institute, 1998.

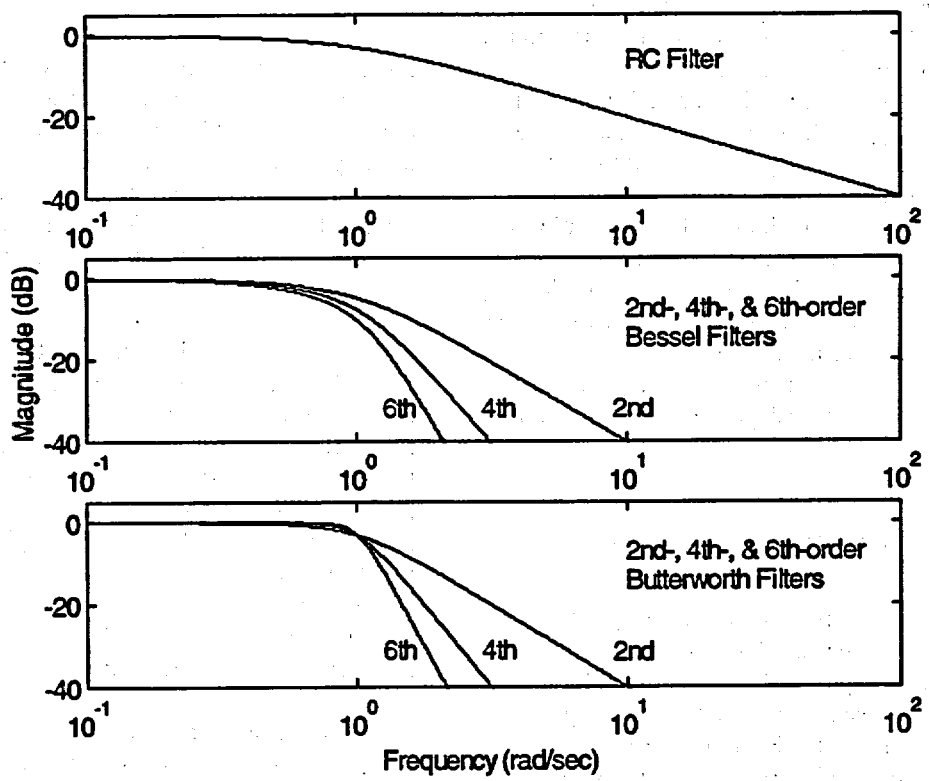


Figure C.2 Frequency responses for the RC, Bessel, and Butterworth filters

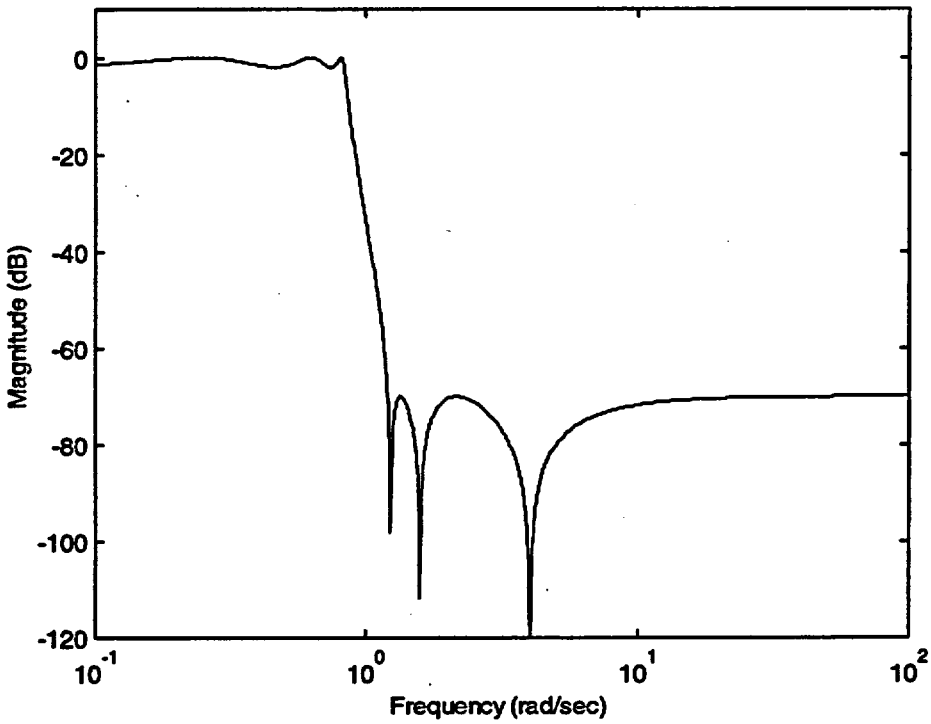


Figure C.3 6-pole/6-zero elliptical filter frequency response

APPENDIX D: OBTAINING THE FREQUENCY SPECTRUM OF A SIGNAL

Finding an input signal's rate of change is necessary for sample rate selection. The rate of change is commonly found using the signal's frequency spectrum. In the early 19th century, Joseph Fourier discovered that a signal could be represented by a sum of sinusoids at various frequencies, with each having its own phase shift and magnitude (Bracewell, 1978; Jackson, 1991). Plots of the sinusoids' magnitude vs. frequency and phase shift vs. frequency form the frequency spectrum. When selecting sample rates, the magnitude vs. frequency plot identifies the highest frequency (rate of change) in the signal and its magnitude. As noted in Chapter 3, this information is used, along with other information, to select a sample rate.

Frequency spectrums are created using a Fourier transform to transform time-domain signals into their sinusoidal components. The time-domain signal is obtained through the actual plant signal, a simulation, or analytical calculation. This appendix describes the advantages and disadvantages of each method, as well as, providing a review of the Fourier transform.

The Fourier Transform

The Fourier transform changes the view of the signal from the time domain to the frequency domain, but it does not change the signal's properties. As mentioned earlier, the frequency-domain view is the frequency spectrum of the signal. It is important to understand how the Fourier transform works to ensure that a correct frequency spectrum is obtained.

The following equation performs the Fourier transform on a signal, x(t):

$$X(j\omega) = \int_{-\infty}^{\infty} x(t) \cdot e^{-j\omega t} dt ,$$

where "ω" represents frequency, "e" is the exponential operator, and "j" is the imaginary operator. This equation assumes a continuous-time signal, and it is not very useful for finding the frequency spectrum of plant signals. For example, if someone is trying to find the frequency spectrum of a pressure signal, it is difficult to find a continuous-time equation, x(t), that would represent that signal. It is easier to obtain discrete data points of the pressure signal and use those points to find the frequency spectrum. The discrete Fourier transform (DFT) takes discrete data points from a time-domain signal, and produces discrete frequency points for the frequency spectrum. The following equation describes the DFT:

$$X[k] = \sum_{n=0}^{N-1} x[n] \cdot e^{-j(2\pi/N)kn} ,$$

where N is the number of discrete data points, X[k] is the set of discrete frequency-domain points, and x[n] is the discrete time-domain points. Even with computers, it can take a considerable amount of time to compute the frequency spectrum with the DFT. There exists a faster method to determine the frequency spectrum for some special cases. This method is the fast Fourier transform (FFT). The steps for the FFT are involved and not listed here. The FFT requires two conditions not required by the DFT. These conditions are:

(1) The number of data points must be 2^n, where n is a positive integer.
(2) The data points must be equally spaced in time (constant sample rate).

Using the DFT/FFT, it appears simple to obtain the frequency spectrum of a signal; especially with various software packages that make the job easier. However, there are some precautions that need to be taken when performing a DFT/FFT. These precautions are covered in the next section.

Frequency Range

The frequency spectrum's frequency range is important. When finding the frequency spectrum of a plant signal, it is necessary to pick up important frequency information. For example, if the potential for embedded noise exists in the signal, it is desirable

to find its frequencies to avoid aliasing. If the frequency range does not extend far enough to capture the noise, it may go unnoticed.

If someone provides N time-domain data points, they receive N frequency-domain data points from the DFT/FFT. When performing the DFT/FFT, both positive and negative frequencies are calculated; one being the mirror image of the other. Only the positive frequencies (N/2 data points) are needed to determine the signal's rate of change. The lowest frequency represented in the frequency spectrum is equal to the reciprocal of the time record length. For example, if data are obtained for a period of 1 second, the lowest frequency represented is 1 Hz. The highest frequency represented is equal to N/2 times the reciprocal of the time record length. Going back to the preceding example, if data points are obtained every 10 milliseconds for a period of 1 second, the highest frequency is 50 Hz. As shown here, the lower frequency range is decreased by taking data points for a longer period of time. The upper frequency range is increased by increasing the sample rate within the period of data collection.

Offsets

For many signals in nuclear facilities, the particular time interval of interest involves a signal starting at a non-zero value and ending up at a different non-zero value. The DFT/FFT algorithms assume the time period of interest is repeating periodically. Figure D.1(a) contains a limited time span plot of pressurizer level in a pressurized water reactor (PWR). Figure D.1(b) illustrates what the DFT/FFT sees. Notice that the sharp discontinuities between each window add high frequency components to the frequency spectrum, which is not a true picture of the original signal (Smith, 1998). Figure D.1(c) is the resulting FFT magnitude plot of the pressurizer level signal.

To avoid placing unwanted high frequencies into the frequency spectrum, it is necessary to remove the discontinuity the DFT/FFT sees. A line, called an anti-offset line, is drawn from the beginning point to the end point of the pressurizer level signal. The anti-offset line is subtracted point by point from the pressurizer level signal. Figure D.2(a) shows the pressurizer level signal with the anti-offset line drawn on top of it, and Figure D.2(b) is the signal after the anti-offset line is subtracted. Other common windowing techniques, such as Hamming and Hanning windows, do not work for this type of signal since it starts and ends at two different values. Hamming and Hanning windows tend to zero out the start and end points.

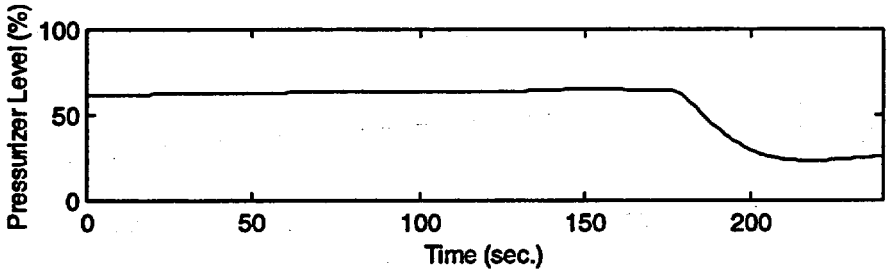
Since the values at the beginning and ending of the window now match at zero, no high frequencies are added. This method reduces the magnitude of some low frequency components, but it should not affect sample rate selection since we are more interested in the magnitude of higher frequencies. Figure D.2(c) shows a large reduction in the magnitude of higher frequencies compared to Figure D.1(c). If the anti-offset line is not used in calculating the frequency spectrum, the sample rate selection is not degraded. Since the offsets increase the magnitude of higher frequencies, they cause the signal to appear to have a faster rate of change, resulting in a more conservative sample rate.

Actual Data Samples

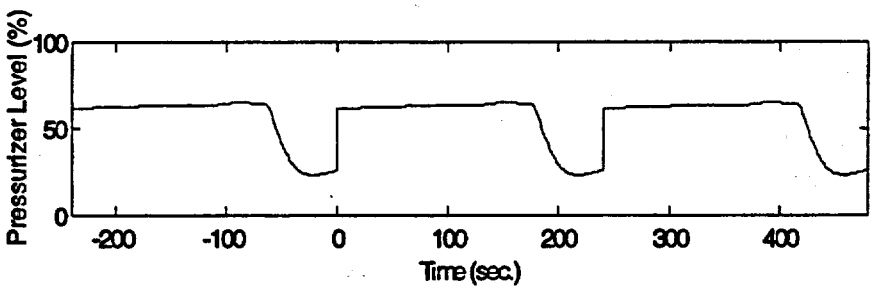
The most direct way to get the data points and calculate the frequency spectrum is to sample the actual plant signal. However, there are two reasons why this is the least feasible method. First, for protection, alarm, and monitoring functions, the greatest demand on the nuclear system occurs for worst-case transients. This data cannot be obtained from an operating plant. Second, it is necessary to sample fast enough to capture, not only the process dynamics, but also the noise making up the total signal entering the digital I&C system. The noise information is necessary to prevent its aliasing.

Simulations

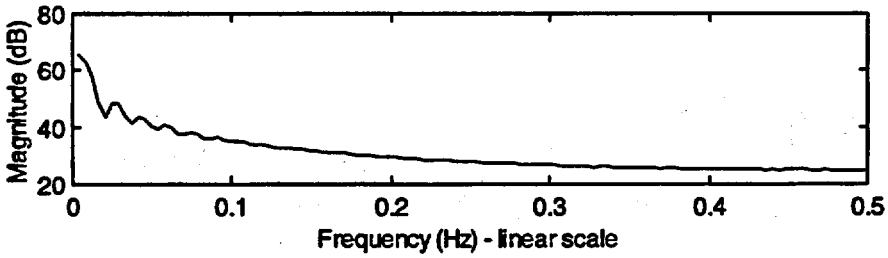
The easiest way to obtain the frequency spectrum is through simulation. If the simulator adequately models the plant dynamics, the time plot of a transient can be obtained. In this case, the data acquisition



(a)



(b)



(c)

Figure D.1 A pressurizer level signal and its frequency spectrum: (a) pressurizer level plot; (b) continuous time-domain signal equivalent used by the Fourier transform; (c) Fourier transform of the equivalent signal

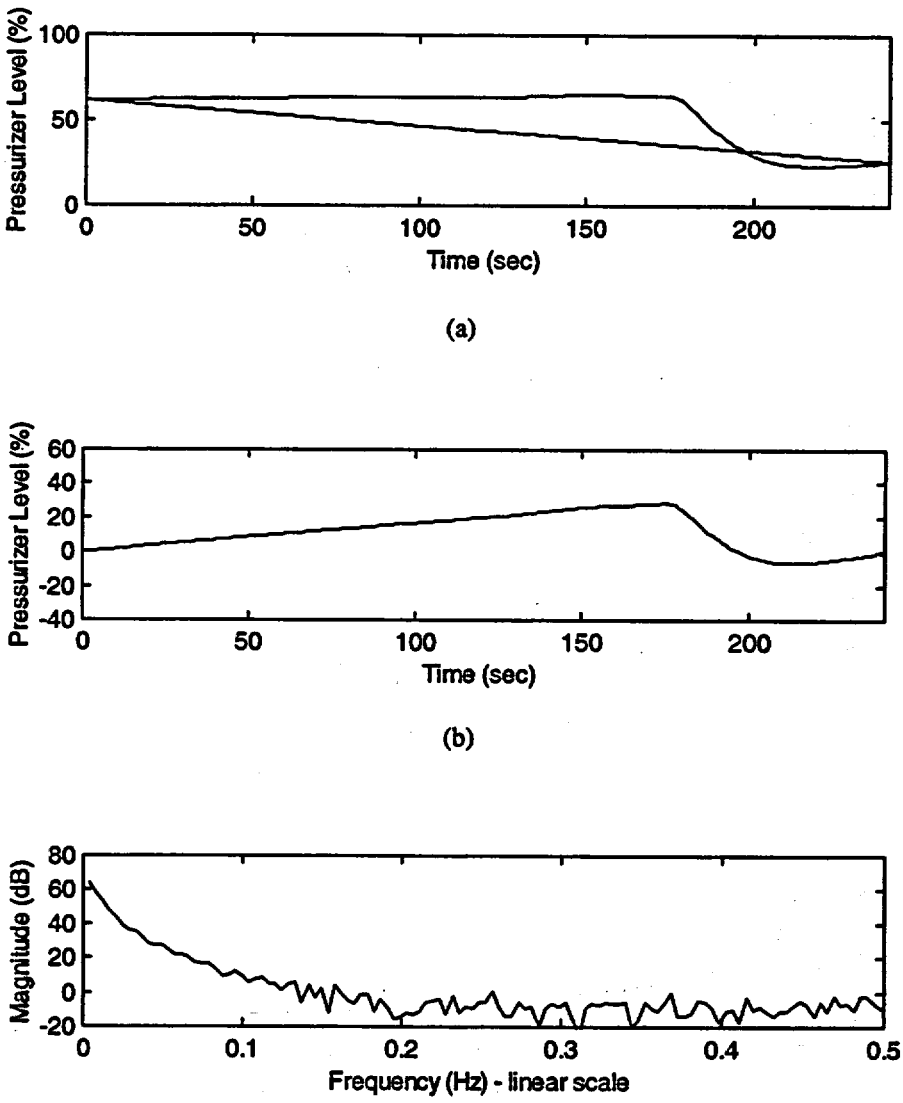


Figure D.2 The modified pressurizer level signal and its frequency spectrum: (a) pressurizer level and the anti-offset line; (b) pressurizer level with the anti-offset line subtracted out; (c) Fourier transform of the modified signal

system needs only to sample fast enough to capture the dynamics of the plant process. Compared to sampling the actual plant signal, this method is less demanding because it is not significantly affected by noise. Because noise does not affect the simulation signal, the simulation provides a good picture of the frequency range of interest. To get an accurate picture of the plant signal, it is necessary to add the noise frequency spectrum to the signal's frequency spectrum. This combination is used to determine the sample rate so that noise, and other unwanted high frequencies, are not aliased in the signal.

Analytical Calculations

Another method to estimate the frequency spectrum of a plant signal is through analytical means. As with simulations, analytical calculations have the advantage of separating the frequency range of interest from unwanted noise. If the largest rate of change is known for a plant signal, it is possible to fabricate an artificial signal that envelopes that rate of change, and calculate the frequency spectrum of the artificial signal. Again, it is necessary to add the signal and noise frequency spectrums together to arrive at a true picture of the actual plant signal. Many control system design techniques use analytical calculations to determine the sample rate.

Spectrum Analyzers

Another way to find the frequency spectrum of a signal is using a spectrum analyzer. A spectrum analyzer finds the magnitude of sinusoids within a signal and plots the magnitude vs. frequency. One must ensure the frequency range for the spectrum analyzer fits the expected frequency range of the signal. Most signals in nuclear power plants are in the low frequency range, falling out of the window of many spectrum analyzers.

References

Bracewell, Ronald N. *The Fourier Transform and Its Applications*, 2nd ed. New York: McGraw-Hill, 1978.

Jackson, Leland B. *Signals, Systems, and Transforms*. Reading, Massachusetts: Addison Wesley, 1991.

Smith, Strether. *Digital Data Acquisition*. Santa Barbara, California: Tustin Technical Institute, 1998.

APPENDIX E: NUCLEAR SAFETY SYSTEM EXAMPLE

Digital sampling introduces error sources not found in analog instrumentation and control (I&C) systems. By not sampling a signal fast enough, high frequencies in an analog signal are represented as low frequencies in the digital signal. This misrepresentation of frequencies is called aliasing. If severe enough, aliasing leads to degraded safety system performance. Therefore, aliasing should be considered alongside other error sources, like amplifier drift, for setpoint calculations. Severe cases of aliasing could cause large deviations between the expected trip point and the actual trip point. However, this is avoidable through proper design techniques.

Appendix E presents three examples related to aliasing and sample delay. The first example uses a pressurized water reactor (PWR) engineered safety features (ESF) trip on high steam flow coincident with low steam pressure, illustrated in Figure E.1. The second example involves the PWR low pressure reactor trip function. The third example describes the impact of reactor trip delay on fuel rod temperature. This appendix not only points to some of the effects digital sampling has on nuclear safety systems, but it also illustrates how sample rate selection is performed using the techniques described in Chapter 3.

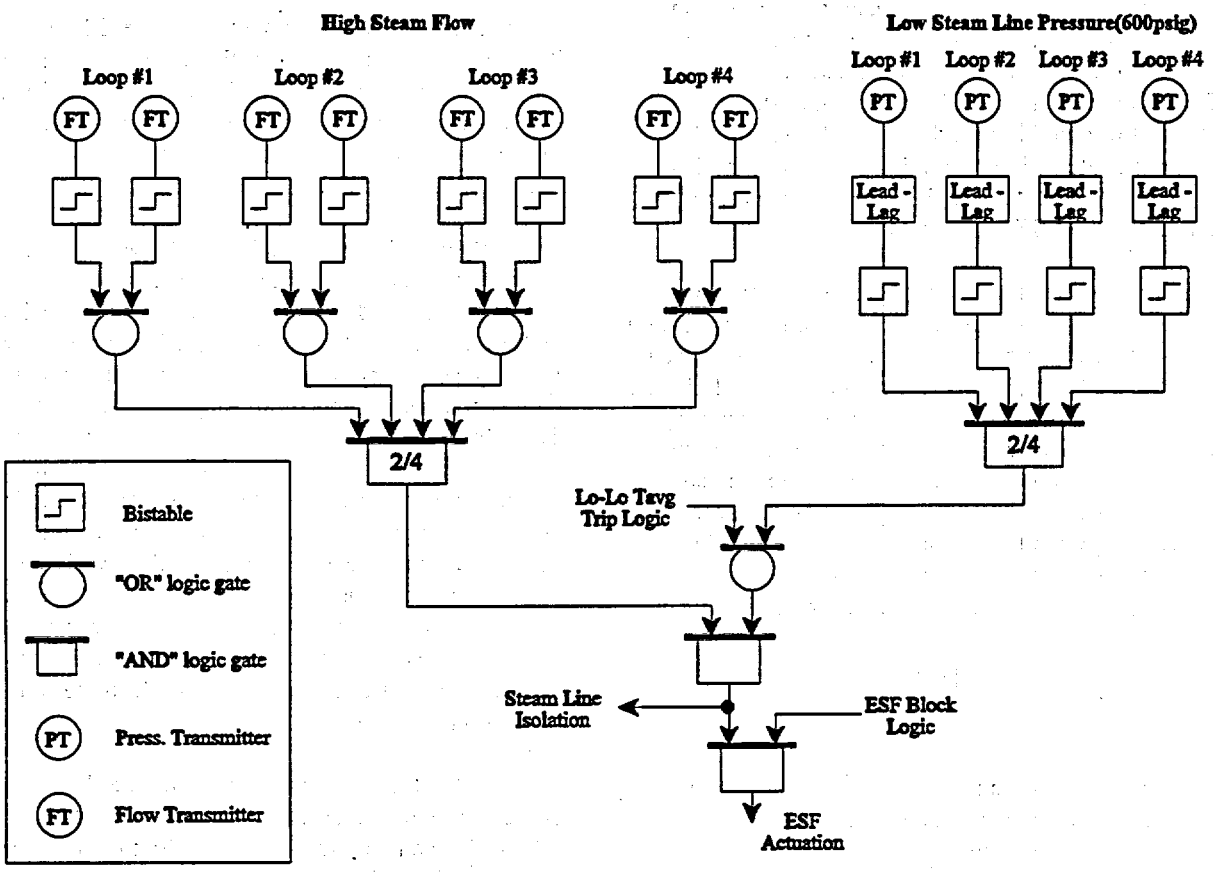


Figure E.1 High steam line flow coincident with low steam pressure ESF trip logic

Example 1: ESF Trip Function

The ESF high steam flow coincident with low steam pressure trip is designed to safeguard fission product barriers from the effects of a steam line break downstream of the main steam isolation valves. Figure E.1 provides the logic diagram for the ESF high steam line flow coincident with low steam pressure trip logic. The diagram represents the analog relay/solid-state safety system typical of many PWRs[1].

In the ESF trip logic, two steam flow signals from each primary coolant loop are processed through a bistable to detect steam flow exceeding a safety setpoint. The safety setpoint for steam flow is a moving setpoint depending upon secondary power. Secondary power is calculated from the first stage turbine pressure. Figure E.2 illustrates the moving high steam flow setpoint for this example. If one of the two bistables in each loop indicates a high steam flow condition, then the "OR" gate indicates a high steam flow condition for that loop. If two out of four loops indicate a high steam flow condition, the 2/4 logic voter indicates a high steam flow condition to the rest of the ESF logic circuitry.

The low steam pressure logic has a stationary setpoint equal to 600 psig. Each signal from the steam pressure transmitter is processed by a lead-lag circuit to make the logic circuit sensitive to the rate of change in pressure. For example, the output of the lead-lag circuit may indicate a steam pressure lower than the low steam pressure setpoint, even though the actual steam pressure is above the setpoint. In such cases, the lead-lag circuit sees a sharp negative trend in steam pressure and anticipates a lower pressure. The lead-lag transfer function for this example is:

$$\frac{1+50s}{1+5s}$$

Two out of four steam pressure transmitters must indicate a low steam pressure condition for the low steam pressure logic to become active.

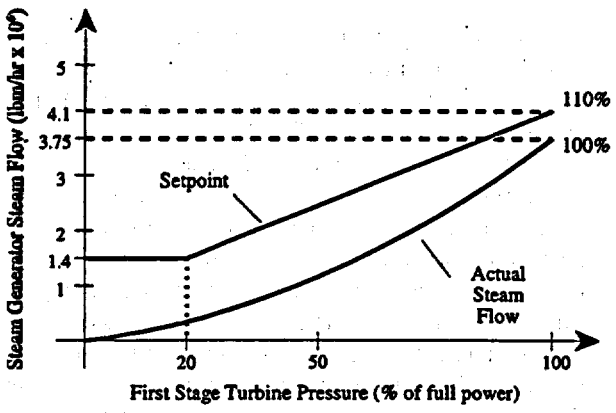


Figure E.2 Setpoint for high steam line flow

Other logic is also present in Figure E.1. The lo-lo Tavg ESF logic output enters the diagram to complete the high steam line flow coincident with lo-lo Tavg. There is also logic to block the ESF actuation for power-up and shut-down of the plant. In this example, these logic items do not come into play.

Only one channel, consisting of one steam line flow transmitter and one steam line pressure transmitter, is used in this example. It is assumed that both of the transmitters work correctly, as well as the ESF logic circuitry. A particular transient is chosen to demonstrate the effects of aliasing on safety systems. This transient involves a hot-leg resistance temperature detector (RTD) failing high at 28% nuclear power. The initial conditions include the steam dumps remaining armed after a previous load rejection. When the transient occurs, the auctioneered high Tavg jumps to a high value due to the failed RTD. Because the steam dumps are already armed, all steam dump valves fully open because of the high Tavg value. Steam flow increases sharply and steam pressure decreases due to the amount of steam being dumped.

The reactor trips on a high steam line flow coincident with low steam pressure ESF actuation. Although steam pressure is ~900 psig, the low steam pressure ESF logic is met because the lead-lag circuit detects a high negative rate for steam pressure and

[1] Data from the USNRC Westinghouse simulator.

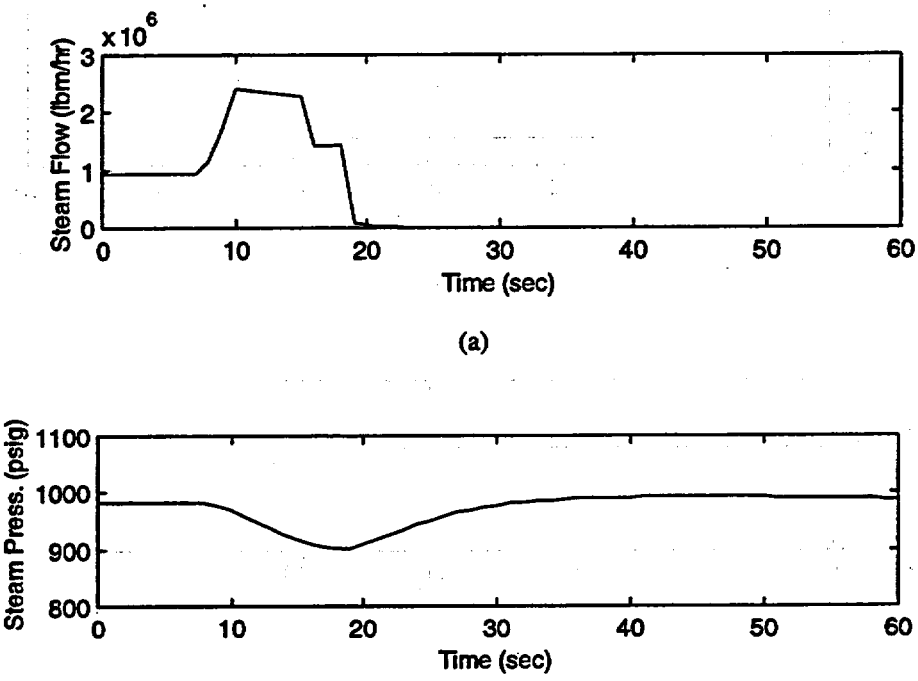


Figure E.3 Failed-high, hot-leg RTD transient response: (a) steam flow; (b) steam pressure

assigns an output value less than 600 psig. The high steam flow logic is met when the steam dumps open fully due to the incorrect auctioneered high Tavg. The analog safety system response from the USNRC Westinghouse simulator is illustrated in Figure E.3. The transient starts 7 seconds into the scenario and the ESF actuation (and thus a reactor trip) occurs at 15.3 seconds.

At the point of reactor trip, steam flow begins decreasing, while the steam pressure begins to increase. If the reactor had not tripped at this point, the steam flow would continue to increase and the steam pressure would continue to decrease. The same rate of change found in the simulator's signals is used to create new input signals for the example. The decreasing steam pressure trend is extended using the same rate of change. The steam flow input signal meets its high steamline flow setpoint limit before steam pressure reaches its setpoint. Therefore, the new steamline flow plateaus at 4.83×10^6 lbm/hr, which is well above the high steamline flow setpoint for 28% nuclear power. Figure E.4 illustrates the input signals for the example.

In actual plant applications, it is important to analyze the most demanding transient for a safety function. The most demanding transient is one that involves the fastest rate of change in the input signal. For instance, the most demanding transient for an ESF low pressurizer pressure trip in a PWR is most likely a large cold leg break since pressure decreases rapidly below the low pressurizer pressure setpoint. The hot leg RTD failing high with the steam dumps already

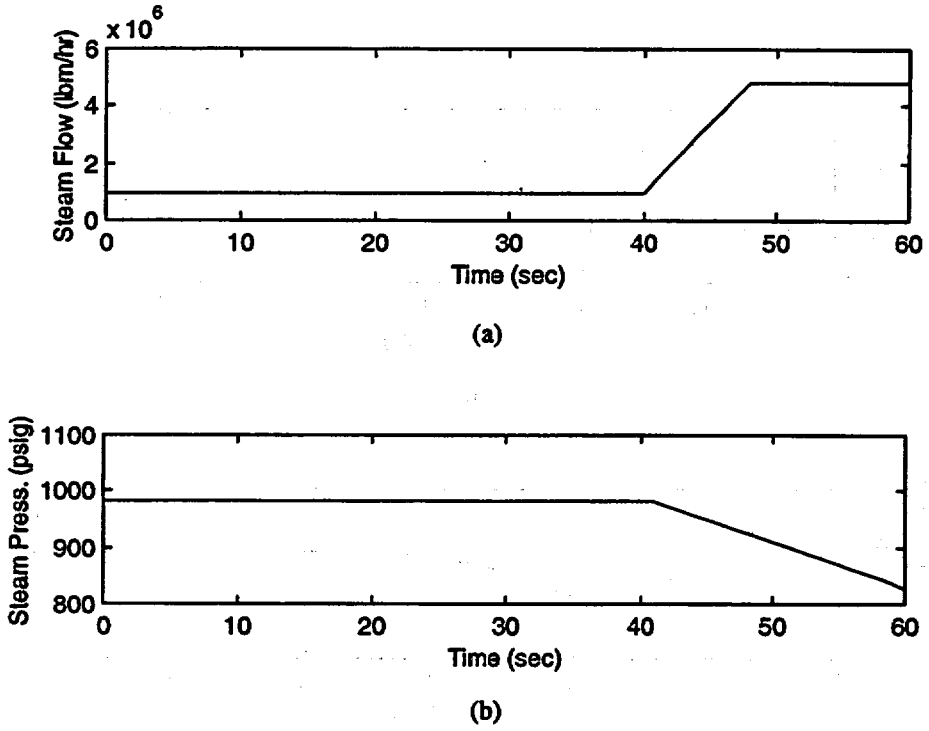


Figure E.4 Transient ramp signals used in the example: (a) steam flow; (b) steam pressure

armed may not be the most demanding transient for the high steam flow coincident with low steam pressure ESF function, but it serves the purpose of demonstrating sample rate problems.

Example 1: Impact of Digital Sampling on the ESF Trip Function

In analog protection systems, trip point accuracy is important. In these protection systems, it is desirable to trip the reactor at a specific pressure, flow, etc. However, due to instrument drift, noise, and other error sources, the actual trip point deviates from the desired trip point. In the past, conservatism was built into the setpoint calculation to account for these errors. With the introduction of digital I&C, some error sources, such as analog drift, are reduced or eliminated. However, digital I&C has its own error sources related to sample rates and computer wordlengths.

The following discussion illustrates the effects of digital sampling on the error between the actual trip point and the desired trip point for a safety channel. Little study has been performed to identify the effects of sampling on digital safety systems. This example only attempts to identify the impact of sample rate selection and to draw general conclusions about the results.

The high steam flow coincident with low steam pressure ESF safety channel is converted from its analog form to a digital form. Figure E.5 on the following page illustrates the setup for the digital safety channel. It is essentially the same as the analog safety channel except for the A/D converters at the steam pressure and steam flow inputs. Also, the lead-lag circuit is transformed to its digital implementation,

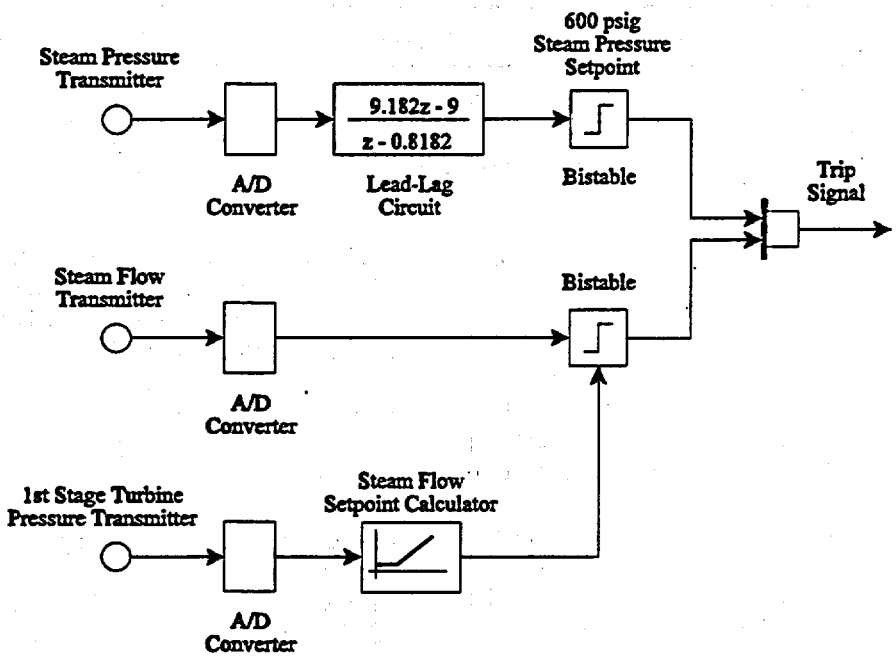


Figure E.5 Single channel, digital safety system used in the example

as noted by the Z-transform in place of the Laplace transform version. The Z-transform is similar to the Laplace transform except it is used for digital systems. Coefficients for the Z-transform lead-lag circuit are dependent upon the sample rate.

To demonstrate the effects of sampling on digital safety systems, three digital versions of the high steamline flow coincident with low steam pressure trip channel are developed. The sample rates for these channels are 0.25 Hz, 0.5 Hz, and 1 Hz. The baseline for the demonstration is the analog protection system response. In the example, the only error sources causing deviations from the desired trip point and the actual trip points is sample delay/ aliasing. When the analog protection system trips, the steam pressure is 907.5 psig and the steam flow is 4.83×10^6 lbm/hr. Table E.1 provides the worst case deviations for the digital safety channels, as compared to the analog results. Since the steam flow is always at its plateau of 4.83×10^6 when the reactor trips, only steam pressure is listed. The percent deviation of the steam pressure from the analog value of 907.5 is listed.

There is an important observation to consider from the preceding demonstration. As the sample rate decreases, the percent deviation from the desired trip point increases. This illustrates the impact of sample delay on setpoint accuracy. Sample rate selection should consider, not only overall response-time requirements, but also consider the sample delay on setpoint accuracy.

Table E.1 Results of varying the sample rate for a digital protection system

Sample Rate	Steam Pressure	Percent Deviation
1 Hz sample rate	891 psig	-1.8 %
0.5 Hz sample rate	881.6 psig	-2.8 %
0.25 Hz sample rate	870.2 psig	-4.1 %

Example 1: Impact of Noise on the Digital ESF Trip Function

This section demonstrates the sampling ratio method of sample rate selection described in Chapter 3. The first requirement is to set an allowable aliasing error bound, which is 1% for this demonstration. Two assumptions of the sampling ratio method are to have the signal's frequency spectrum constant or trending downward, and the cutoff frequency of the anti-aliasing filter equal to the bandwidth frequency of the signal. Both of these conditions are met in the example.

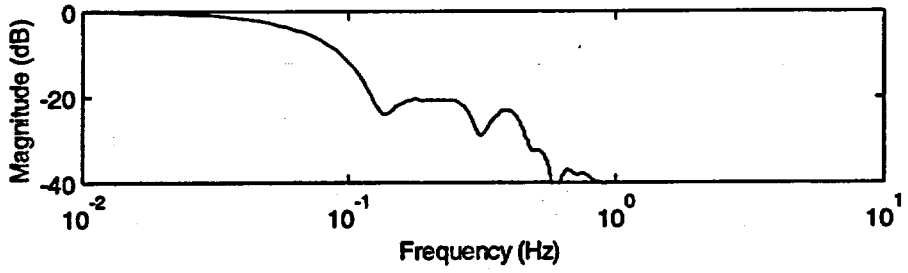
To determine the sample rate for a safety channel, the frequency spectrum is calculated for the worst-case transient involving that safety function. This frequency spectrum is illustrated in Figure E.6. It was determined in the previous example that steam pressure is the most limiting variable for the high steamline flow coincident with low steam pressure ESF function. Therefore, its frequency spectrum is considered in selecting a single sample rate for both steam flow and pressure signals. To meet the 1% allowable aliasing error requirement, it is necessary to capture all the information in frequencies with gain above -40 dB (0.01). Using the normalized frequency spectrum of Figure E.6(b), the frequency corresponding to -40 dB for steam pressure is 3.9 Hz. Therefore, the steam pressure signal bandwidth for this transient is 3.9 Hz.

The third and final requirement is the selection of an anti-aliasing filter. In this example a fourth-order Butterworth filter is arbitrarily chosen. Using Table 3.2 in the main text, a 4-pole Butterworth anti-aliasing filter allowing 1% aliasing error has a sampling ratio of 4.1. The required sample rate is equal to the sampling ratio times the signal bandwidth: 4.1×3.9 Hz = 15.99 Hz, or approximately 16 Hz. The sample period is the inverse of the sample rate, which is 0.0625 second. The sample period is approximated to 0.06 second.

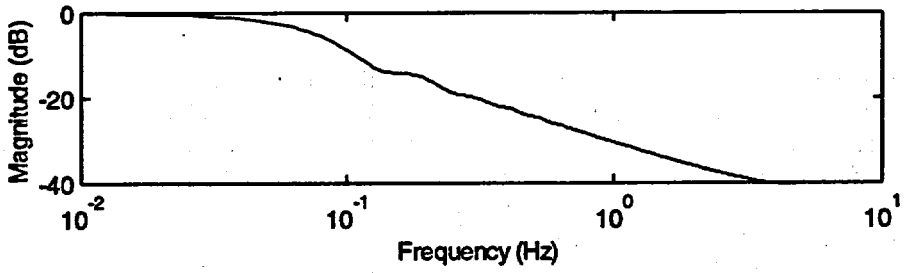
Using the calculated sample rate, 100 tests are run to demonstrate the effectiveness of the sampling ratio method. In the setup, two different noise sources are added to the input signal to produce, at maximum, 1% full-scale error of the input signal. The input signals are represented by a voltage range of 0 to 10V. Therefore, the maximum noise magnitude is 0.1 V. One noise source is uniform random noise with a maximum and minimum value of 0.1 and -0.1, respectively. The other noise source is a 60 Hz sine wave with an amplitude of 0.1.

The digital protection channel test results are provided in Table E.2. The table shows results for the channel without noise, with uniform random noise, and with 60 Hz noise. Each scenario considers two cases; one using an anti-aliasing filter and one that does not use an anti-aliasing filter. Both the worst-case trip point and the best-case trip point from the trials are presented. With each case, the steam pressure and the percent deviation of the steam pressure from the 907.5 psig desired trip point are given.

In the no-noise trial, the digital safety system with the anti-aliasing filter performs worse than the digital safety system without the filter for two reasons. The



(a)



(b)

Figure E.6 The magnitude frequency spectrum of (a) steam flow and (b) steam pressure for the RTD failed-high transient example

Table E.2 Results of digital sampling in the presence of noise

Noise		Worst Case		Best Case	
		Steam Pressure	% Deviation	Steam Pressure	% Deviation
No Noise	No Anti-aliasing Filter	903.3 psig	-0.5%	903.8 psig	-0.4%
	With Anti-aliasing Filter	897.9 psig	-1%	898.4 psig	-1%
Uniform Random Noise	No Anti-aliasing Filter	825.5 psig	-9%	938.7 psig	+3.4%
	With Anti-aliasing Filter	896.5 psig	-1.2%	896.9 psig	-1.2%
60 Hz Noise	No Anti-aliasing Filter	830.4 psig	-8.5%	936.9 psig	+3.2%
	With Anti-aliasing Filter	897.9 psig	-1%	898.4 psig	-1%

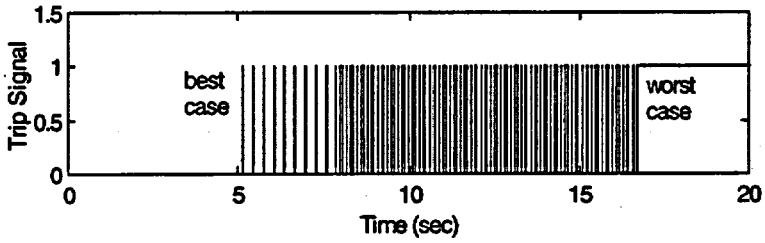


Figure E.7 Typical trip signal received from channels subjected to noise without anti-aliasing filters

anti-aliasing filter attenuates high frequencies, while the lead-lag tends to strengthen them. Therefore, the two components work against each other. Even though the digital safety system with the anti-aliasing filter has a larger trip point deviation, it is still with the 1% allowable error criterion. Also, the anti-aliasing filter adds time delay to the signal.

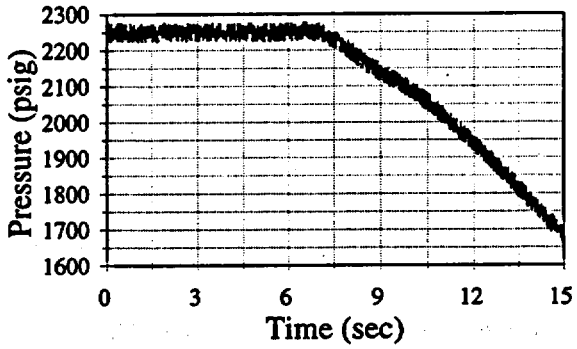
The digital safety channels performed similarly when subjected to uniform random and 60 Hz noise. In cases in which there is no anti-aliasing filter, the channel bounces between the tripped and untripped states until it settles to the tripped state. Figure E.7 illustrates the trip signal received from the digital safety channels without an anti-aliasing filter, where the value "1" equals the tripped state. For digital safety systems without anti-aliasing filters, the worst-case deviation refers to the point at which the trip value eventually settles to the tripped state. The best-case value, for the same set of tests, depicts the moment when the first trip signal is received. Note that the deviation is to the conservative side. If a digital safety channel locks in the first trip signal it receives, then the safety channel, for this particular example, would trip in a conservative manner.

When digital safety channels with anti-aliasing filters were subjected to uniform random and 60 Hz noise, they performed at or near their performance level in the absence of noise. The case with uniform random noise has a deviation slightly over 1%, and this is mainly due to the low frequency portion of the uniform random noise passing through the anti-aliasing filter. If noise is within the bandwidth of an anti-aliasing filter, it will pass through unattenuated. These results illustrate the capability of anti-aliasing filters to reduce aliasing problems and maintain required trip point accuracy. Also, the anti-aliasing filters provide a more consistent trip pattern.

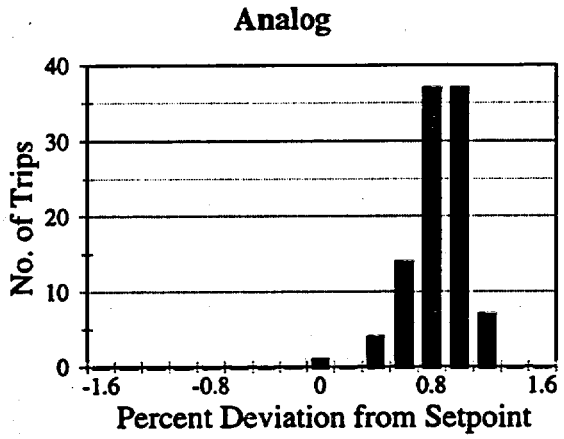
Example 2: Low Pressure Reactor Trip Function

Example 2 uses the low pressurizer pressure reactor trip function for a PWR to illustrate the impact of sample rate selection. Using data from the USNRC's Westinghouse simulator, the setpoint pressure for the low pressure reactor trip is 1865 psig, and the transient is a six-inch cold leg break occurring seven seconds into the scenario. The pressure signal for this transient contains uniform random noise with a magnitude of 2% peak-to-peak, of full-scale value (2500 psig). Figure E.8(a) illustrates the pressure signal. For comparative purposes, the trip point is observed for three types of protection channels. The first protection channel is analog, the second channel is digital with a sample rate of 20 Hz, and the third channel is digital with a sample rate of 10 Hz. Each channel is exercised with one hundred trials, and none use an AAF.

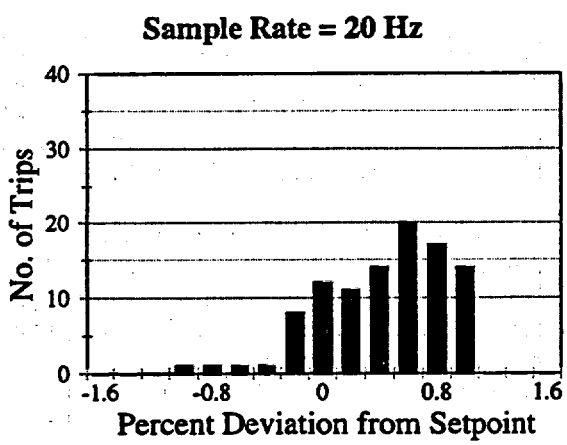
Figures E.8(b), E.8(c), and E.8(d) illustrate the percent deviation of the trip point from the setpoint for the analog, 20 Hz-sampling, and 10 Hz-sampling channels. Table E.3 provides the averages and variance for the data collected. A positive deviation indicates the channel trips before the setpoint is



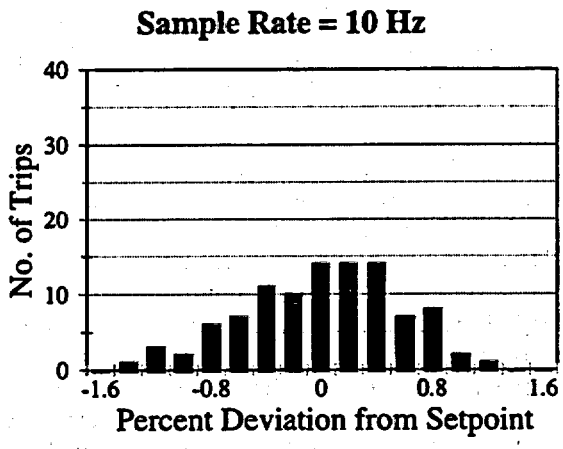
(a)



(b)



(b)



(d)

Figure E.8 Comparison of low pressurizer pressure setpoint deviations for three protection channels: (a) pressurizer pressure signal with noise; (b) percent deviation distribution for an analog channel; (c) percent deviation distribution for a 20 Hz-sampling digital channel; (d) percent deviation distribution for a 10 Hz-sampling digital channel.

Table E.3 Averages and variances for the pressurizer pressure trip point deviation experiment

Protection Channel Type	Average Deviation from Setpoint	Variance
Analog	0.94%	0.04%
20-Hz Sampling	0.53%	0.19%
10-Hz Sampling	0.1%	0.29%

reached, which is caused by the noise riding on the signal. In all three channels, the average percent deviation is positive, but the analog channel is the most conservative in this respect. Also, the analog channel has less variance compared to the digital channels. As the sample rate decreases in the digital channels, the trip data increases in variance. Both observations suggest an impact on setpoint calculation due to sample rate selection. The sampling ratio method for sample rate selection is now applied to the same experimental setup.

Example 2: Sample Rate Selection for the Reactor Trip Function

The following steps illustrate sample rate selection for the digital, low pressure reactor trip function. The sampling ratio method, which is described in Chapter 3, is used to determine the sample rate.

Step 1: For the purposes this example, less than 1% accuracy error is desired in the input signal. To achieve the 1% error requirement, all frequencies in the pressure signal whose magnitude contribute more than 1% of the total signal must be included in the bandwidth. A normalized frequency spectrum of the pressure signal is calculated using a Fast Fourier Transform. The bandwidth frequency is identified as the frequency corresponding to -40dB, which is equal to 7 Hz. A 6-pole Butterworth filter is selected as the AAF, and its frequency response is provided in Figure E.9(a). The cutoff frequency for the AAF is set equal to the bandwidth frequency, F_D, which is 7 Hz. The uniform random noise in the pressure signal does not introduce magnitudes above -40 dB for frequencies beyond F_D.

Step 2: Since the accuracy error should be less than 1%, and (in this case) the only error source is aliasing, the allowable aliasing error is equal to 1%. To find the frequency for required aliasing attenuation, F_R, a horizontal line is drawn at the value corresponding to -40 dB(1%). Figure E.9(a) illustrates this horizontal line. F_R is equal to the frequency corresponding to the intersection of the frequency response and horizontal line. This frequency value is 16 Hz.

Step 3: The sample ratio, SR, is equal to: $1 + (F_R/F_D) = 1 + (16/7) = 3.3$. The sample rate is then equal to: $SR \times F_D = 3.3 \times 7$ Hz = 23.1 Hz. The sample period is equal to: 1/sample rate = 0.043 seconds. This value has been approximated to 0.05 seconds.

Using the calculated sample rate and selected AAF, a digital protection channel is subjected to one hundred trials using the pressurizer pressure signal in the previous experiment. Figure E.9(b) illustrates the percent trip point deviation from the setpoint. The histogram shows the 1% aliasing error requirement is met for all trials. With an average percent deviation of -0.6%, the digital channel trips non-conservatively. The non-conservative trip point deviation is due to the following reasons. First, the noise causing the conservative trips in the previous experiments is greatly reduced by the AAF. Second, the AAF slightly delays the signal reaching the trip logic. Third, the sampling action also delays the signal. Despite the non-conservative trip aspect, this digital channel shows more predictability in the trip point as noted by a variance of 0.02%.

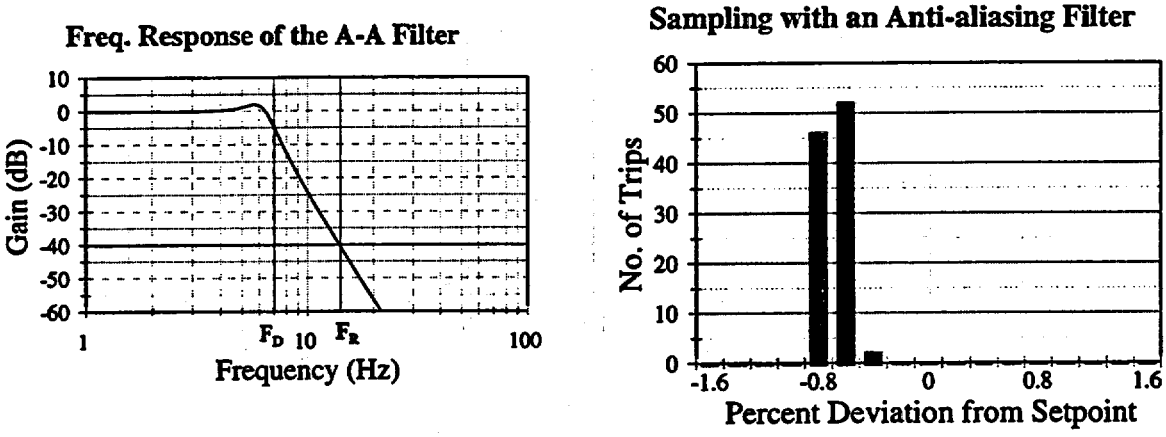


Figure E.9 Sample rate calculation: (a) frequency response of the anti-aliasing filter; (b) percent deviation distribution using the calculated sample rate

Example 3: Impact of Sampling Delay on Fuel Rod Temperatures

Reactor protection systems act within a specified amount of time to limit the damage to the fuel cladding. Any delays in reactor protection system actuation may cause fuel cladding temperatures to rise; possibly to the point of cladding oxidation at some portions of the fuel. Response time requirements of reactor protection systems are specified to limit the amount of fuel cladding oxidation. A double-ended cold-leg break for the AP600 nuclear power plant illustrates the change in fuel cladding temperature for delay in reactor trip[2]. Figure E.10(a) illustrates the impact of delaying a reactor protection system trip by a certain number of seconds. Figure E.10(b) provides the actual reactor trip time for a given delay, where the first possibility of a trip is 1.5 seconds into the transient.

The simulation results shown in Figure E.10 illustrate the impact of sample delay on a reactor protection system. For this case, the transient requires quick action from the reactor protection system to avoid fuel cladding damage. A delay of 1 second by the reactor protection system causes an approximate 30 K rise in fuel cladding temperature. Other transients or protection systems may not be impacted by long sampling delays due to the lower severity of the transient, or the rate of change of the measured variable. Small sampling delays (below 1 second) should not appreciably affect fuel cladding temperature.

Conclusions

The examples offered in this appendix display the effects of sampling on nuclear safety systems. As the sample rate decreases, digital safety channels suffer from more sample delay/aliasing and result in increased deviation form the desired trip point. The required sample rate is dependent on the rate of change of the analog input signal, as well as the amount of allowable aliasing. It has been demonstrated that anti-aliasing filters are effective against signal noise, and the sampling ratio method is a viable sample rate selection method. Also, sampling causes delay in safety-related systems, and this delay has an impact on fuel cladding protection. However, the amount of tolerable delay is dependent on the type of transient and the protective function.

2 TRAC-M/F77 simulation of a double-ended cold-leg break for an AP600 plant.

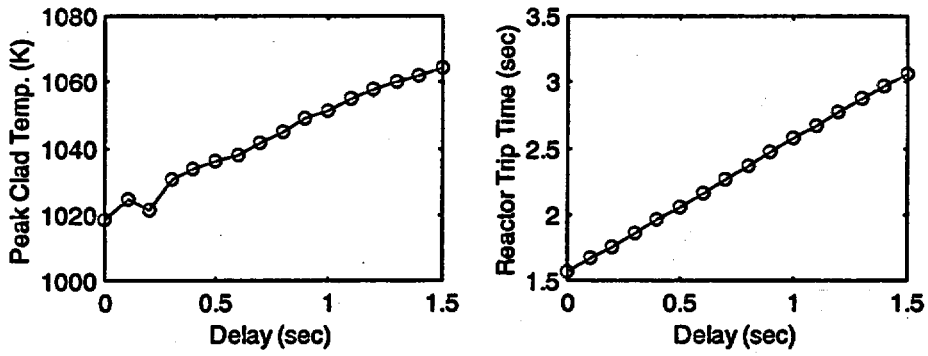


Figure E.10 Impact of time delay on fuel cladding temperature: (a) peak cladding temperature; (b) reactor trip time

When reviewing digital safety systems, it is important to remember three things. First, where does the safety channel trip and how far is the actual trip point from the desired trip point? Does the setpoint error fall within allowable tolerances? Does the digital safety channel meet response-time requirements? These issues are the same as those in dealing with analog protection systems, only aliasing and sample delay are new sources of error.

Reference

USNRC. *Westinghouse Technology Systems Manual.* Washington, D.C.: U. S. Nuclear Regulatory Commission, 1998.

APPENDIX F: NUCLEAR CONTROL SYSTEM EXAMPLE

Digital control system performance is impacted by sample rate selection. Sampling adds delay to control systems, decreasing their stability margin (Franklin et al., 1990). However, proper design and sample rate selection minimize sampling effects on control system performance. Appendix F (1) demonstrates a sample rate selection method for a control system, (2) demonstrates the effect of sampling on control systems, and (3) provides comments for nuclear control system reviews.

Appendix F meets these objectives through an example of a steam generator water level control system. The example does not model any plant in particular, but the system layout is typical of many pressurized water reactors (PWRs).

The Steam Generator Water Level Control System

The steam generator water level control system is a prime candidate for digital upgrades because of difficulties in controlling water level at low power levels and the impact this control system has on plant operation (Miossec et al., 1980; Irving et al., 1980). The flexibility and promise of digital control algorithms can enable robust control over the entire operating range.

Figure F.1 illustrates a typical steam generator water level control system (Miossec et al., 1980). This system is a non-minimum phase system since the steam

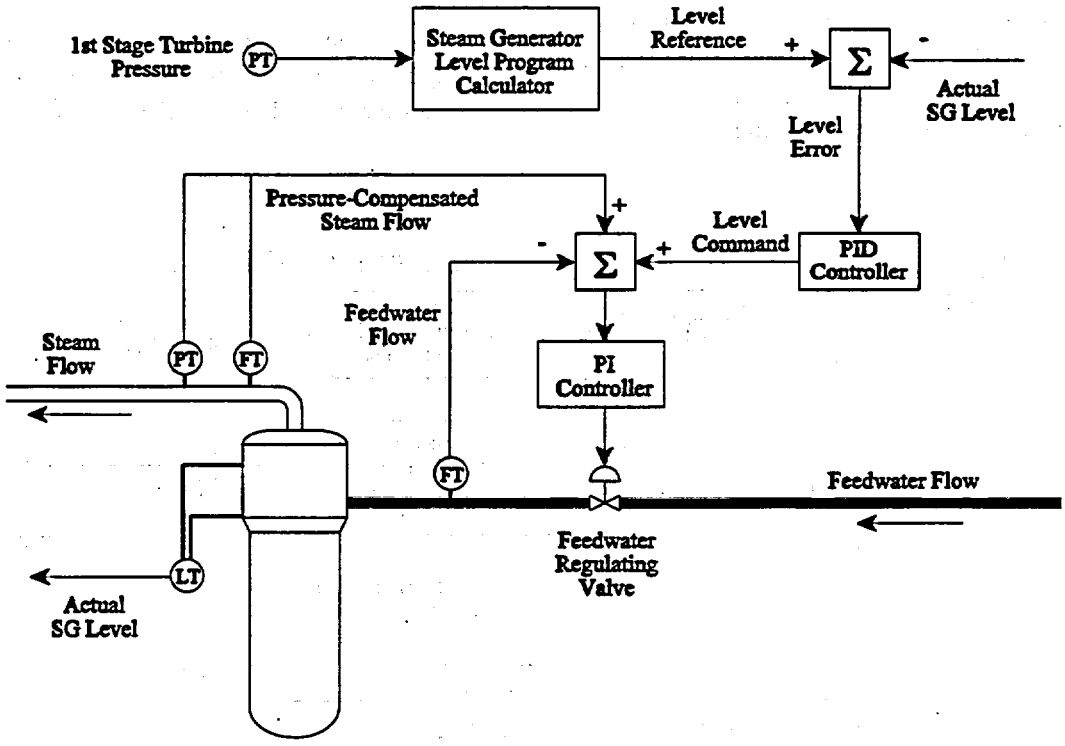


Figure F.1 The steam generator water level control system

generator water level initially reacts in the opposite direction of its final value for a given transient (shrink-and-swell effect). When PWRs were first built, analog PID and PI controllers were used. For comparison's sake, the steam generator water level control system response using analog control is analyzed as a benchmark against the digital control response.

Figure F.2 provides the control system block diagram for the steam generator water level control system. The structure of the steam generator transfer function model is taken from the work of Miossec, Tassart, and Irving (Miossec et al., 1980; Irving et al., 1980). The steam generator transfer function is a fourth-order model, and the feedwater regulating valve is a first-order model. These transfer functions, along with the controllers and other components, are tuned to match the response of the USNRC's Westinghouse simulator for a particular operating condition. That operating condition is an 11% load decrease from 100% power in a 50 second time period. The models do not need to be accurate to the simulator's response since the digital control system performance is benchmarked against the analog control system performance. However, care has been taken to make the models as realistic as possible. The only changes between the analog and digital control simulation is the digitization of the PI and PID controllers.

The steam generator water level control system is a multiple-loop system, with the feedwater regulating valve control loop comprising the inner control loop, as shown in Figure F.2. The outer control loop comprises the entire steam generator water level control system, including the feedwater regulating valve control system. References to inner and outer control loops are used in the rest of the appendix. Both loops have their own closed-loop frequency response, and their controllers use different sample rates.

Determining the Sample Rate

As noted in Chapter 3, one way to select the sample rate for a control system is the closed-loop bandwidth method. Figure F.3(a) provides the a

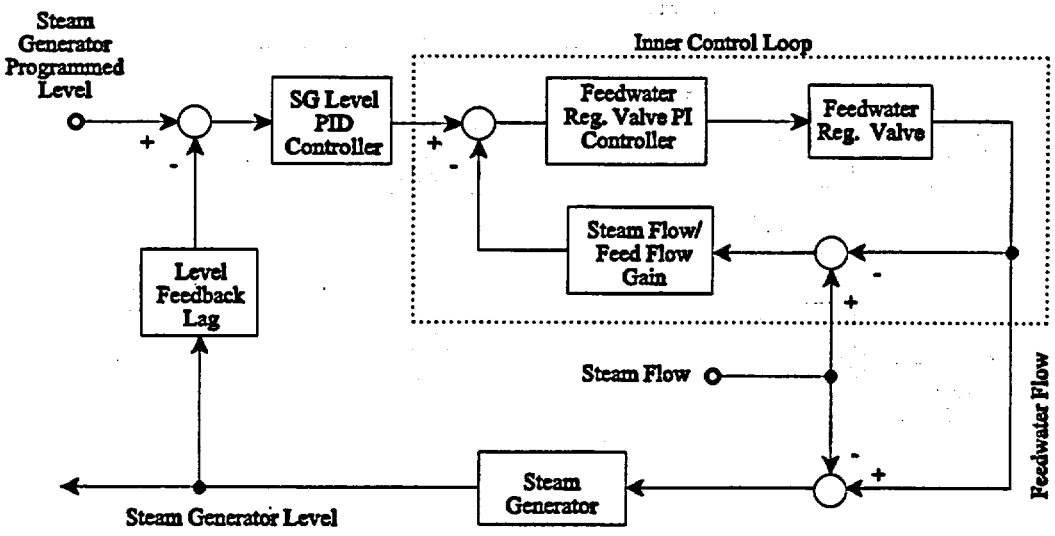
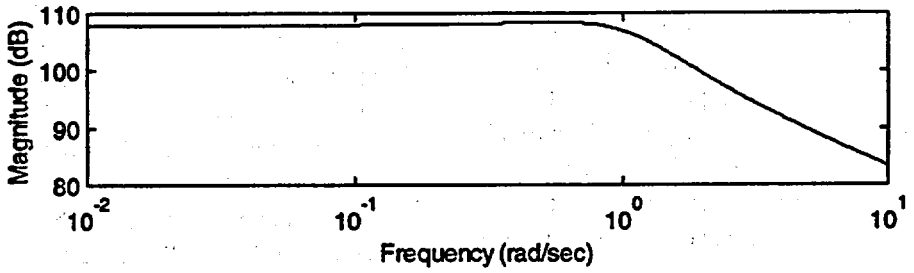
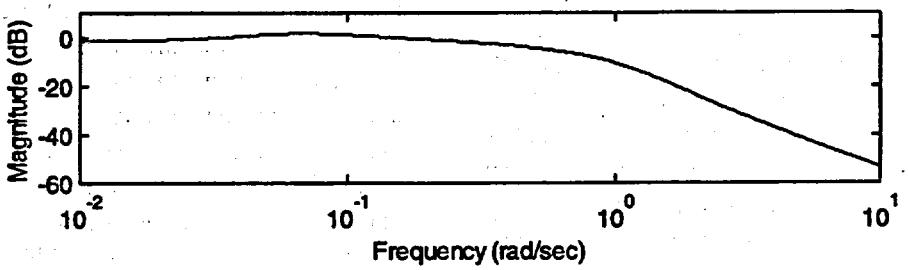


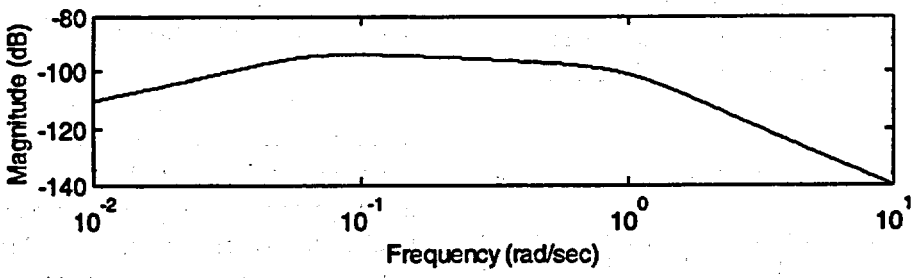
Figure F.2 Block diagram for the steam generator level control system



(a)



(b)



(c)

Figure F.3 The magnitude frequency response for: (a) the inner control loop, (b) the outer control loop (programmed level is the input), and (c) the outer control loop (steam flow is the input)

closed-loop frequency response for the inner control loop. Figure F.3(b) provides the outer control loop frequency response with respect to steam generator programmed level input, and Figure F.3(c) provides the outer control loop frequency response with respect to the steam flow input. Because the outer control loop has two inputs (programmed level and steam flow), there are two frequency response plots. It is important to obtain the frequency response plots for all input-output relationships. A second frequency response is not needed for the steam flow input to the inner control loop because there is only a gain between the two input points.

The closed-loop bandwidth for the inner and outer control loops is determined from the magnitude frequency responses. The bandwidth is commonly defined as the frequency where the magnitude is 3 dB below the DC gain (magnitude at zero frequency) (Nise, 1992). Frequencies below the -3 dB point have no more than half the power of the DC gain frequency. This definition works fine for systems whose frequency magnitudes are monotonically decreasing. But, for systems whose magnitude frequency plots are not monotonically decreasing, such as the one in Figure F.3(c), the DC gain may be substituted for the maximum, or near-maximum gain in the magnitude frequency plot. Table F.1 provides the bandwidth for the three frequency responses shown in Figure F.3.

Table F.1 Bandwidths of the frequency responses

Control Loop	Bandwidth	
	rad/sec	Hz
Inner Control Loop	1.26	0.2
Outer Control Loop — Programmed Level	0.38	0.06
Outer Control Loop — Steam Flow	1	0.16

The Digital Control System

Conversion from analog to digital control is fairly straightforward and methods are given in most digital control textbooks. A critical specification requires the DC gain of the analog and digital controllers to match. For this example, conversion from analog to digital control is fairly straightforward. The same gains used for analog control are used for digital control since the DC gain does not change. Both the PI feedwater regulating valve controller and the PID steam generator level controller are digitized.

The sample rate for a controller is based on the closed-loop bandwidth for the loop it controls. The inner control loop of Figure F.2 has a bandwidth of 0.2 Hz, and the outer control loop's bandwidth is 0.16 Hz (the highest bandwidth of the two inputs). In this example, three digital control versions are implemented. The sample rates for the PID and PI controllers are calculated in each version by multiplying the inner and outer control loop bandwidths by 2.5, 5, and 10. Table F.2 provides the sample rate for the PID and PI controllers.

The Effects of Digital Sampling

Converting from analog to digital control often results in different control system responses due to the sampling (Franklin et al., 1990). Figure F.4 on the next page demonstrates the steam generator water level control system response to an 11% steam demand decrease from 100% power, over 50 seconds. The analog control system response to this transient is the benchmark to evaluate the digital control system response. The analog response is illustrated in all three digital control system time response plots.

One important observation is that the digital control systems approach a more oscillatory response as the sample rate decreases. Eventually, it becomes

Table F.2 Steam generator water level response to a 11% load decrease

Sample Rate Selection	Sample Rate		Time Response	
	Inner-loop	Outer-loop	% Overshoot	Settling Time
Analog Control	n/a	n/a	6%	107 sec
10x Bandwidth	0.5 sec	0.62 sec	3%	94 sec
5x Bandwidth	1 sec	1.25 sec	6%	100 sec
2.5x Bandwidth	2 sec	2.5 sec	13%	374 sec

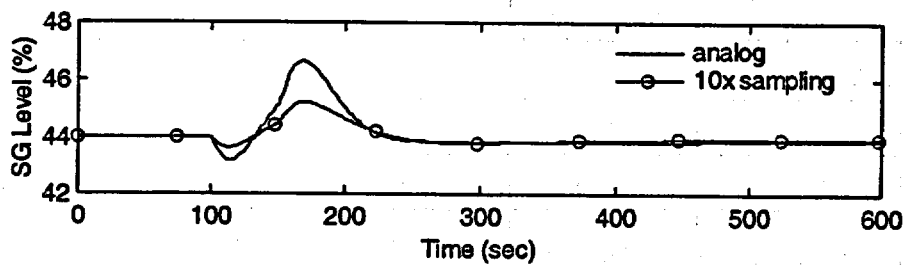
unstable. This phenomenon is common in digital control systems (Franklin et al., 1990; Nise, 1992). There is a small, but nevertheless significant difference in the 5x and 10x response as indicated in Figure F.4(a) and (b). Increasing sample rates may not provide significant performance enhancement beyond a certain point. Other factors, such as computer capability and finite wordlength issues, should also be considered when sampling very fast.

The response corresponding to the 5x and 10x sample rate provides a better response than the analog control system. Normally, the analog control system response outperforms the digital response provided they execute the same basic control algorithm. Sampling moves the poles and zeros of a control system, adding undesirable properties such as reduced gain/phase margin. In this particular example, sampling sampling moves the transfer function zero in a manner that reduces the shrink-and-swell effect.

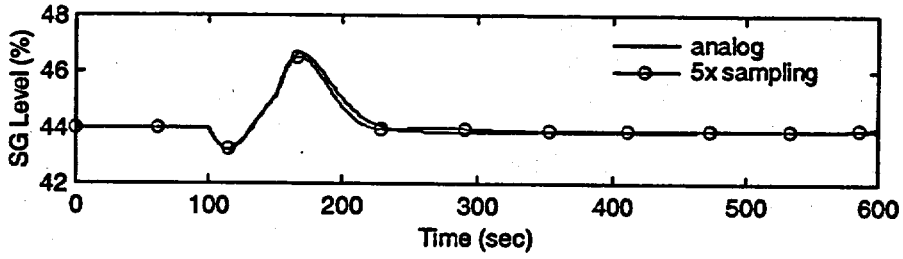
Other tests show that the theoretical minimum sample rate for both the PI and PID controllers is not achievable. The theoretical minimum sample rate is just above twice the closed-loop frequency bandwidth. Table F.3 provides the actual and predicted sample rates just before instability is reached. These results show that, while the 2x bandwidth rule is a good benchmark for starting sample rate selection, it is not conservative. For real applications, the sample rate should be several times higher than the theoretical 2x bandwidth limit. This is especially true for systems experiencing large amounts of signal noise or nonlinearities. The closed-loop bandwidth is a good starting point, but it is necessary to sample at least 6 to 10 times faster than that bandwidth (Franklin et al., 1990).

Table F.3 Actual and predicted sample rates/periods before instability

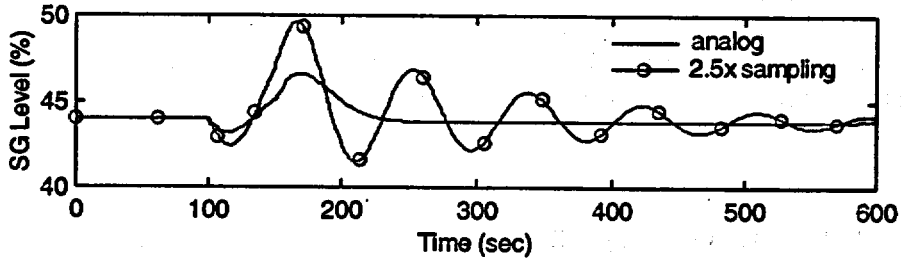
	Predicted		Actual	
	Sample Period	Sample Rate	Sample Period	Sample Rate
Inner Control Loop	2.5 sec	0.4 Hz	2.2 sec	0.45 Hz
Outer Control Loop	3.1 sec	0.32 Hz	2.8 sec	0.36 Hz



(a)



(b)



(c)

Figure F.4 Comparison of analog and digital control system response with sample rates equal to (a) 10x the closed-loop bandwidth, (b) 5x the closed-loop bandwidth, and (c) 2.5x the closed-loop bandwidth

Reviewing Control Systems

When reviewing digital control systems, it is important to look at the system's time response to several expected transients. If the time response is highly oscillatory, then the sample rate may be a problem. In this situation, try to compare the digital control system response to an analog control system response. The digital control system may oscillate slightly more than its analog counterpart, but the oscillatory behavior should not present a potential safety hazard.

This example did not consider signal noise, but in real applications, it is necessary to deal with noise through noise minimization techniques (e.g., anti-aliasing filters). Other methods, such as the gain/phase margin and rise-time method are also able to determine the necessary sample rate.

Summary

The primary aspect of sampling and digital control is stability. As demonstrated in this example, conversion from analog to digital control can lead to different control system responses. For decreasing sample rates, the digital control system response becomes more oscillatory. The oscillations are caused by sampling delay, which reduces the phase margin of the control system. This example demonstrates the necessity of sampling 6 to 10 times faster than the closed-loop bandwidth.

This example used the closed-loop bandwidth method, but other methods, such as the rise time and phase/gain margin method, could be used for sample rate selection. As this example illustrates, sampling faster reduces oscillations. However, the example does not consider other factors, such as computer capability and finite wordlength issues, which may adversely affect performance when sampling extremely fast.

References

Franklin, G., J. Powell, and M. Workman. *Digital Control of Dynamic Systems*, 2nd ed. Reading, Massachusetts: Addison-Wesley, 1994.

Irving, E., C. Miossec, and J. Tassart. "Towards efficient full automatic operation of the PWR steam generator with water level adaptive control," *Boiler Dynamics and Control in Nuclear Power Stations 2*. London: British Nuclear Energy Society, 1980.

Miossec, C., J. Tassart, and E. Irving. "Automatic control of steam generator levels in EDF PWR units," *Boiler Dynamics and Control in Nuclear Power Stations 2*. London: British Nuclear Energy Society, 1980.

Nise, Norman S. *Control Systems Engineering*. Redwood, California: The Benjamin/Cummings Publishing Co., 1992.

NRC FORM 335 (2-89) NRCM 1102, 3201, 3202

U.S. NUCLEAR REGULATORY COMMISSION

BIBLIOGRAPHIC DATA SHEET

(See instructions on the reverse)

1. REPORT NUMBER (Assigned by NRC, Add Vol., Supp., Rev., and Addendum Numbers, if any.)

NUREG-1709

2. TITLE AND SUBTITLE

Selection of Sample Rate and Computer Wordlength in Digital Instrumentation and Control Systems

3. DATE REPORT PUBLISHED

MONTH	YEAR
July	2000

4. FIN OR GRANT NUMBER

5. AUTHOR(S)

T. W. Jackson

6. TYPE OF REPORT

Technical

7. PERIOD COVERED *(Inclusive Dates)*

8. PERFORMING ORGANIZATION - NAME AND ADDRESS *(If NRC, provide Division, Office or Region, U.S. Nuclear Regulatory Commission, and mailing address; if contractor, provide name and mailing address.)*

Division of Engineering Technology
Office of Nuclear Regulatory Research
U.S. Nuclear Regulatory Commission
Washington, DC 20555-0001

9. SPONSORING ORGANIZATION - NAME AND ADDRESS *(If NRC, type "Same as above"; if contractor, provide NRC Division, Office or Region, U.S. Nuclear Regulatory Commission, and mailing address.)*

Same as above

10. SUPPLEMENTARY NOTES

11. ABSTRACT *(200 words or less)*

Digital sampling of analog signals adds two types of errors, aliasing and finit e wordlength error, to the sampled version of the signal. Aliasing is characterized by high frequency components misrepresented as low frequency components in the sampled signal. It is greatly influenced by the sample rate, and may lead to degraded performance in monitoring, alarm, control, and protection systems. Since computer wordlengths are finite in length, digital s ystems are limited in their capability to represent real number values. Finite wordlength errors related to round-off, truncation, and data conversion have the potential to adversely impact the performance of digital instrumentation and control (I&C) s ystems.

The Office of Nuclear Regulatory Research is investigating good engineering pra ctices and review guidance regarding aliasing and finite wordlength errors in nuclear facilities. Hazards associated with th ese errors are minimized through proper design and selection of sample rates and computer wordlengths. This document provides the regulatory background, theoretical information, practical issues, best engineering practices, and examples associa ted with sample rate and computer wordlength selection. This information is used by NRC staff to identify improper treatmen t of aliasing and finite wordlength error in digital I&C systems.

12. KEY WORDS/DESCRIPTORS *(List words or phrases that will assist researchers in locating the report.)*

Analog-to-Digital Converters, Accuracy, Calibration, Calibration Standards, Com puters, Data Acquisition, Data Processing, Digital Filters, Digital Frequency Analysis, Digi tal Systems, Digital-to-Analog Converters, Electronic Equipment, Errors, Frequency Analysis, Reactor Instrumentation, Reactor Protection Systems, Real Time Systems, Resolution, Sig nal-to-Noise Ratio, Time Delay, Time Resolution, Time Series Analysis, Tolerance

13. AVAILABILITY STATEMENT

unlimited

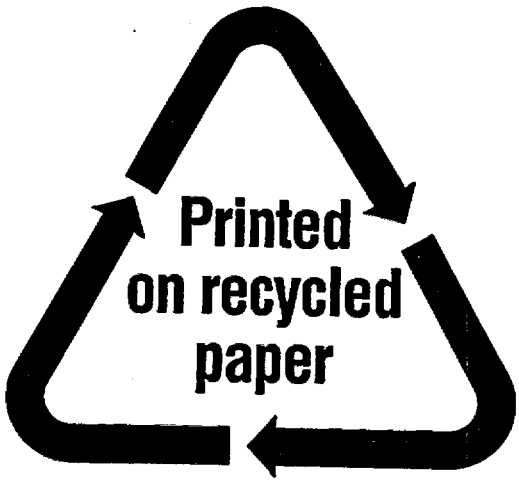
14. SECURITY CLASSIFICATION

(This Page) unclassified

(This Report) unclassified

15. NUMBER OF PAGES

16. PRICE



Federal Recycling Program

UNITED STATES
NUCLEAR REGULATORY COMMISSION
WASHINGTON, D.C. 20555-0001